

## Product Features

Frequency: DC ~ 6GHz

Gain: 20.5dB@1.6GHz

Psat: 38dBm@1.6GHz

PAE: 67%(Pout=38dBm, 1.6GHz)

V<sub>DD</sub> Supply Voltage 28V, static Supply Current  
100mA

Package: QFN24 (4mm×4mm)

## Application

Power Amplification Stage for Wireless

Infrastructure

Test and Measurement Equipment

Commercial and Military Radars

Universal Transmitters and Jammers

Ultrashort Wave Communication Equipment

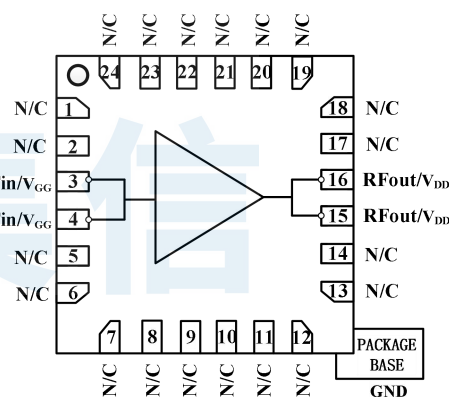
## Ordering Information

| Part Number   | Package | Description                       |
|---------------|---------|-----------------------------------|
| BRGM060006FPJ | QFN24   | DC ~ 6GHz<br>GaN Power Transistor |

## General Description

The BRGM060006FPJ is a Gallium nitride (GaN) wideband transistor with a +28V drain supply that achieves 6W (37.8dBm) of power output in a DC to 6GHz bandwidth with a power added efficiency (PAE) of up to 67%. The high efficiency, high gain, and wide bandwidth characteristics of the BRGM6FPJ make it a strong application in both linear and compressed amplifier circuits, while also simplifying link design and related heat consumption management.

## Functional Block Diagram



## Absolute Maximum Ratings

| Parameters                                 | Values         |
|--------------------------------------------|----------------|
| Gate drain breakdown voltage ( $BV_{DG}$ ) | 100V           |
| Gate pressure range ( $V_{GG}$ )           | -6 to 0V       |
| Drain current ( $I_D$ )                    | 1.1 A          |
| Gate current ( $I_G$ )                     | 2mA            |
| Continuous dissipated power ( $P_D$ )      | 25W            |
| Channel temperature ( $T_{CH}$ )           | 275 °C         |
| Welding climb temperature (30 seconds)     | 245 °C         |
| Storage temperature                        | -65°C ~ +150°C |
| Operating temperature                      | -55°C ~ +85°C  |

Note: The absolute maximum rating indicates the limit value that the device can withstand, exceeding the absolute maximum rating may cause permanent damage to the device. Working under absolute maximum rating conditions for a long period of time will affect the reliability of the device. Please pay attention to good heat dissipation under high temperature operation.

## Recommended Operating Conditions

| Parameters                                | Values        |
|-------------------------------------------|---------------|
| Drain voltage ( $V_{DD}$ )                | +28V (Typ)    |
| Drain static current ( $I_{DQ}$ )         | 100mA (Typ)   |
| Gate voltage ( $V_{GG}$ )                 | -2.52V (Typ)  |
| Channel temperature ( $T_{CH}$ )          | 225 ° C (Max) |
| Continuous power dissipation CW ( $P_D$ ) | 20W (25 ° C)  |

Note: Power amplifier tube electrical specifications are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

### Impedance Mismatch

| Signs | Parameters                  | Typ. |
|-------|-----------------------------|------|
| VSWR  | Impedance mismatch strength | 5:1  |

Test conditions: DEMO board test, =  $T_A$  25°C,  
 $V_{DD}$  =+28V,  $I_{DQ}$  =100mA, Freq=1GHz, CW wave,  
 = $P_{out}$ 6W test;

### Thermal Parameters

| Parameters                           | Test Conditions   | Value | Units |
|--------------------------------------|-------------------|-------|-------|
| Thermal resistance ( $\theta_{JC}$ ) | Dc at 85 ° C case | TBD   | °C/W  |

Note:  $\theta_{JC}$  to measure the thermal resistance to the bottom of the exposed pad;

### ESD Warnings



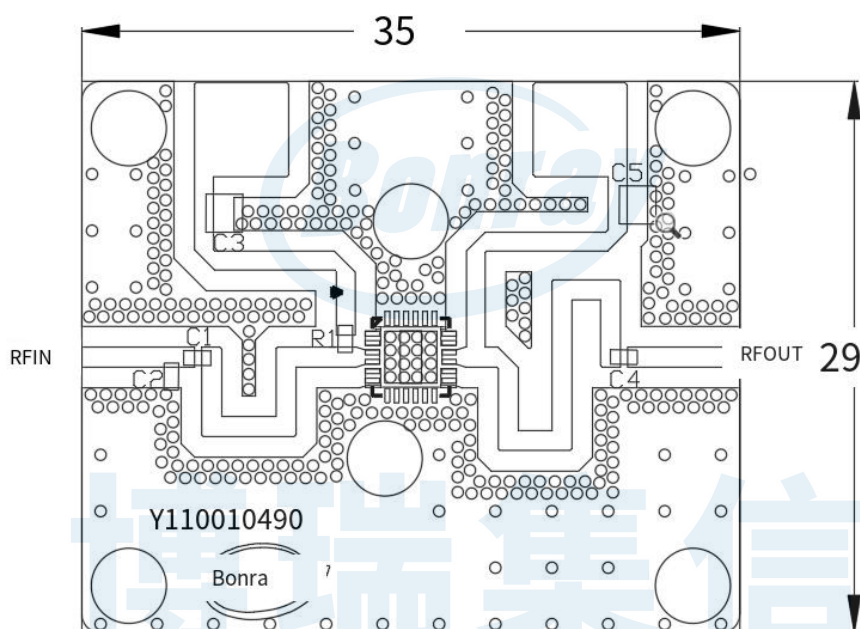
**ELECTROSTATIC SENSITIVE DEVICE**  
**OBSERVE HANDLING PRECAUTIONS**

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**Option 1: EVB Test Data (1.2GHz ~ 2.2GHz,  $V_{DD}=28V$ ,  $I_{DQ}=100mA$ , single tone signal)**

| Frequency                | 1200 | 1300 | 1400 | 1500  | 1600 | 1700 | 1800  | 1900 | 2000  | 2100 | 2200 | MHz |
|--------------------------|------|------|------|-------|------|------|-------|------|-------|------|------|-----|
| Gain                     | 20.8 | 20.9 | 21.1 | 21.2  | 21.4 | 21.5 | 21.5  | 21.4 | 21.0  | 20.4 | 19.5 | dB  |
| Pout ( dBm ) @ $P_{sat}$ | 38.2 | 38.6 | 38.8 | 38.7  | 38.7 | 38.9 | 38.9  | 38.5 | 38.2  | 38.1 | 38.7 | dBm |
| Power gain @ $P_{sat}$   | 13.7 | 14.1 | 14.4 | 14.25 | 15.3 | 15.5 | 16.45 | 17.2 | 15.85 | 15.7 | 15.3 | dB  |
| PAE@ $P_{sat}$           | 49.4 | 51.8 | 55.2 | 54.0  | 55.0 | 57.4 | 59.5  | 57.1 | 54.6  | 54.4 | 58.9 | %   |

**Typical Application Schematic**



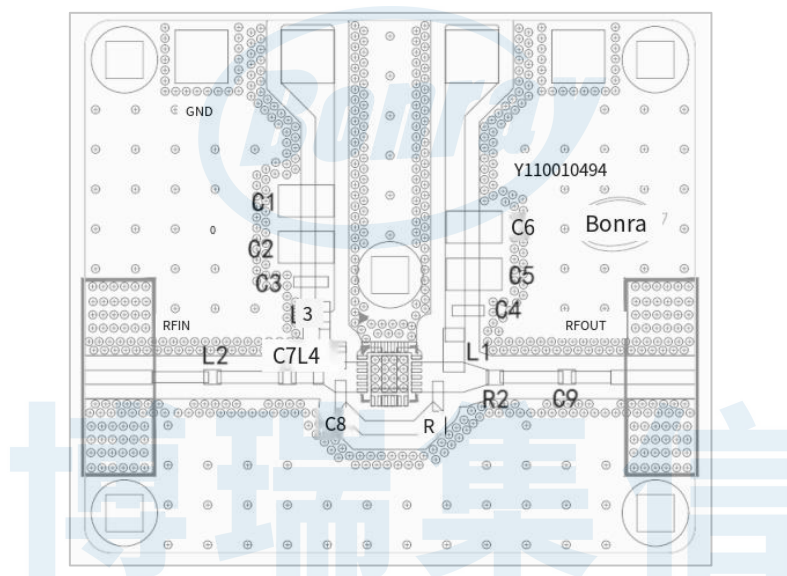
**Bill of Material**

| Reference Designator | Value | Specifications       |
|----------------------|-------|----------------------|
| C1, C4               | 18pf  | 0603 package, high Q |
| C2                   | 1pf   | 0603 package, high Q |
| C3, C5               | 10uf  | 1210 package, 100V   |
| R1                   | 50ohm | 0603 Package         |

**EVB Test Data (30MHz ~ 700MHz,  $V_{DD}=28V$ ,  $I_{DQ}=15mA$ , single tone signal)**

| Frequency (MHz) | 30    | 70    | 100   | 200   | 300   | 400   | 512   | 600   | 700   | MHz |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-----|
| IP1             | 20.1  | 20.1  | 20.2  | 20.3  | 20.6  | 20.9  | 21.3  | 21.4  | 22.1  | dBm |
| OP1             | 36.9  | 37.0  | 37.2  | 37.2  | 37.3  | 37.4  | 37.3  | 36.8  | 37.0  | dBm |
| NF              | 3.5   | 2.2   | 2.2   | 1.5   | 1.5   | 1.3   | 1.4   | 1.6   | 1.8   | dB  |
| S21             | 17.8  | 17.9  | 18.0  | 17.9  | 17.7  | 17.5  | 17.0  | 16.4  | 15.9  | dB  |
| S11             | -7.4  | -7.3  | -7.3  | -7.3  | -7.4  | -7.0  | -6.5  | -5.8  | -5.0  | dB  |
| S22             | -11.0 | -11.5 | -11.4 | -11.6 | -11.5 | -11.6 | -11.5 | -11.2 | -10.7 | dB  |
| PAE@OP1         | 51.8% | 51.9% | 54.3% | 55.3% | 53.6% | 55.2% | 53.4% | 49.6% | 50.5% | %   |

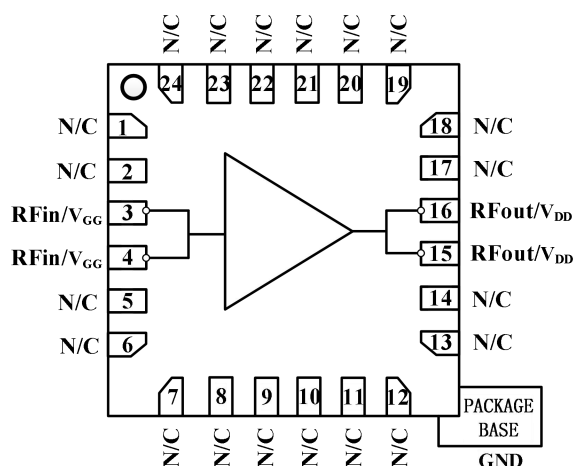
**Typical Application Schematic**



**Bill of Material**

| Reference Designator | Value        | Specifications |
|----------------------|--------------|----------------|
| C1,C2,C5,C6          | 10uF         | 1210           |
| C3,C4                | 10nF         | 0603           |
| C7                   | 1nF          | 0603           |
| C9                   | 3.3 the nF   | 0603           |
| C8                   | 180pF        | 0603           |
| L1                   | 1.1 uH       | 1008           |
| L2                   | 18nH         | 0603           |
| L3                   | 560nH        | 0603           |
| L4                   | 560nH        | 0603           |
| R1                   | 820 $\Omega$ | 0603           |
| R2                   | 0 $\Omega$   | 0603           |

## Pin Configuration and Description



| Pin Number           | Pin Name              | Description                                                                  |
|----------------------|-----------------------|------------------------------------------------------------------------------|
| 3,4                  | RFin/V <sub>GG</sub>  | Transistor gate, gate voltage regulation, RF signal 50Ω system input;        |
| 15,16                | RFout/V <sub>DD</sub> | Transistor drain, drain voltage input, RF power signal 50Ω system output;    |
| 1,2,5 to 14,17 to 24 | N/C                   | No internal connection, but all indicators are tested with N/C pin grounded; |
| -                    | Package Base          | Ground substrate, to be welded to the board card, to ensure good grounding;  |

### Power-on Sequence

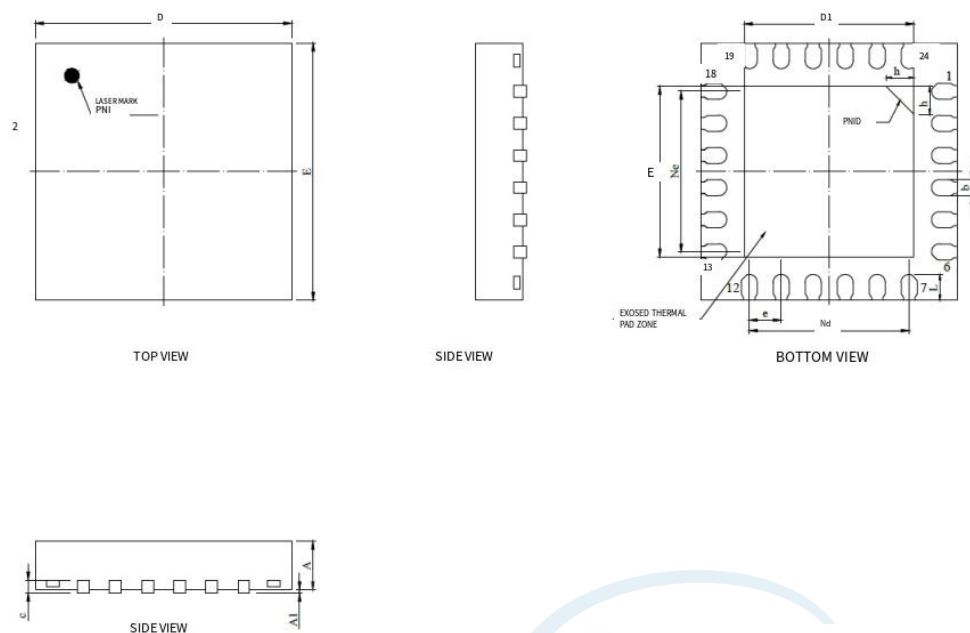
1. Set the gate voltage ( $V_{GG}$ ) to -5V, current limit 10mA;
2. Set drain voltage ( $V_{DD}$ ) to +28V, current limit 2A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage ( $V_{GG}$ ) so that the drain current is 100mA;
6. Input RF signal;

### Power-off Sequence

1. Turn off the RF signal;
2. Reduce the gate voltage ( $V_{GG}$ ) to -5V;
3. Turn off the drain Supply Voltage voltage;
4. Turn off the gate Supply Voltage voltage;

Note: When the circuit is designed, the offset voltage needs to have a timing protection circuit to ensure that it is fully powered on before adding, and ensure that it is reduced to below 5V when powering off, before starting to power off;  $V_{GG}V_{DD}V_{DD}V_{GG}$  Especially in TDD Application, gate Supply Voltage decoupling capacitors need to be rigorously evaluated to meet switching speed requirements.

## Package Dimensions (mm)



| SYMBOL | MILLIMETER |      |      |
|--------|------------|------|------|
|        | MIN        | NOM  | MAX  |
| A      | 0.70       | 0.75 | 0.80 |
| A1     | —          | 0.02 | 0.05 |
| b      | 0.20       | 0.25 | 0.30 |
| c      | 0.203REF   |      |      |
| D      | 3.90       | 4.00 | 4.10 |
| D1     | 2.60       | 2.70 | 2.80 |
| e      | 0.50BSC    |      |      |
| Ne     | 2.50BSC    |      |      |
| Nd     | 2.50BSC    |      |      |
| E      | 3.90       | 4.00 | 4.10 |
| E1     | 2.60       | 2.70 | 2.80 |
| L      | 0.35       | 0.40 | 0.45 |
| h      | 0.30       | 0.35 | 0.40 |

## Recommended Soldering Temperature Profile

