Product Features

Output Frequency Range：25.5MHz～3.24GHz

Fractional-N Frequency Synthesizer

Low Power：122mW

Programmable 1/2/4/8/16/32/64 frequency division output

Supply Voltage：1.8V、2.5V

Dual-Modulus Prescaler：4/5、8/9

SPI Output

Package：QFN24（4mm*mm）

Operating Conditions

Digital Supply Voltage DVDD_LST：2.5V

Digital Supply Voltage DVDD_DIG：1.8V

Analog Supply Voltage AVDD_VCO1：2.5V

Analog Supply Voltage AVDD_BUFF/AVDD_DIV/ AVDD_PFD/AVDD_PRE/AVDD_CP/AVDD_VCO2/AVDD_VCO3/ AVDD_VCO4：1.8V

Operating Temperature：-55℃~+125℃

Storage Temperature：-65℃~+150℃

Storage Temperature：-65℃~+150℃

Ordering Information

Table 1. Ordering Information

Part Number	Package	Description
BR9068FPJ	QFN24	Fractional-N PLL with Integrated VCO PLL

General Description

BR9068FPJ is a low-power frequency synthesizer (PLL) product. Combined with an external loop filter and an external reference clock, BR9068FPJ can implement fractional-N or integer-N phase-locked loop (PLL) frequency synthesizer functionality. This product typically operates with a supply current of 47 mA at 1.8 V and 15 mA at 2.5 V. Compared to the BR9179 product, it consumes slightly more power while optimizing phase noise performance at offsets ≥100 kHz from the carrier, making it equally suitable for low-power application scenarios.

BR9068FPJ integrates a voltage-controlled oscillator (VCO) with a fundamental output frequency range of 1.62 GHz to 3.24 GHz. Through 1/2/4/8/16/32/64 frequency division circuits, it can generate RF output frequencies as low as 25.5 MHz. All on-chip registers are controlled via a standard serial peripheral interface.

Functional Block Diagram

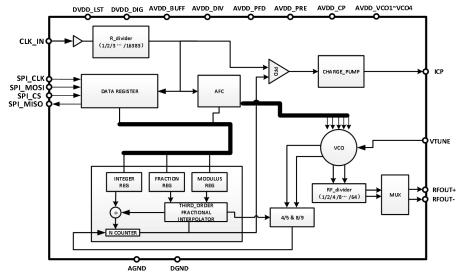


Figure 1. Functional Block Diagram

Specifications（Unless otherwise specified，AVDD_BUFF=AVDD_DIV=AVDD_PFD=AVDD_PRE=AVDD_CP= AVDD_VCO2=AVDD_VCO3=AVDD_VCO4=DVDD_DIG=1.8V±10%，AVDD_VCO1=2.5V±10%，DVDD_LST=2.4V~3.6V。Operating Temperature：T_A=-55℃~+125℃。）

Table 2. Electrical Characteristics

Parameters		Test Conditions	Minimum value	Typical value	Maximum value	Units
Input Reference Characteristics	Input Frequency	-	-	-	600	MHz
	Input Sensitivity		0.4	-	1.8	Vp-p
PFD	PFD Frequency	-	5	-	10	MHz
CP	Current	0.3V≤CPOUT≤1.3V	0.32	-	6.08	mA
	charge-discharge current mismatch		-	1	-	%
	I_{CP} vs. VTUNE		-	1.5	-	%
	I_{CP} vs. Temperature		-	2	-	%
Logic Inputs	Input High VoltageV	-	2.4	2.5	3.6	V
	Input Low VoltageV	-	0	-	0.4	V
Logic Outputs	Output High VoltageVOH	-	2.4	-	3.6	V
	Output Low VoltageVOL		0	-	0.4	V
Supply	DVDD_LST	-	2.4	2.5	3.6	V
	AVDD_VCO1		-	2.5	2.63	V
	AVDD_BUFF=AVDD_DIV=AVDD_PFD=AVDD_PRE=AVDD_CP=AVDD_VCO2=AVDD_VCO3=AVDD_VCO4=DVDD_DIG	-	-	1.8	2	V
	Supply Current	CLK_IN=10MHz prescaling ratio=1、Ndivision ratio=200、VCO output division ratio=1	-	47@1.8V	-	mA
			-	15@2.5V	-	mA
RF Output Characteristic	VCO Output Frequency	-	1620	-	3240	MHz
	VCO Sensitivity KVCO	-	-	100	-	MHz/V
	Minimum RF Output Power	Temperature：25℃ RFOUT+/ RFOUT-	-	0.9	-	dBm
	Maximum RF Output Power		-	4.3	-	dBm
	Minimum VCO Tuning Voltage	-	-	0.3	-	V

	Maximum VCO Tuning Voltage	-	-	1.3	-	V
Phase-Noise Performance	VCOPhase-Noise Performance @1.62GHz	10 kHz Offset	-	-67	-	dBc/Hz
		100 kHz Offset	-	-106	-	dBc/Hz
		1 MHz Offset	-	-130	-	dBc/Hz
	VCOPhase-Noise Performance @3.24GHz	10 kHz Offset	-	-61	-	dBc/Hz
		100 kHz Offset	-	-97	-	dBc/Hz
		1 MHz Offset	-	-123	-	dBc/Hz
	PLL Phase-Noise Performance@1.62GHz PFD Frequency：10MHz Loop Bandwidth：60KHz	1 kHz Offset	-	-94	-	dBc/Hz
		10 kHz Offset	-	-90	-	dBc/Hz
		100 kHz Offset	-	-103	-	dBc/Hz
		1 MHz Offset	-	-130	-	dBc/Hz
	PLL Phase-Noise Performance@3.24GHz PFD Frequency：10MHz Loop Bandwidth：60KHz	1kHz Offset	-	-89	-	dBc/Hz
		10 kHz Offset	-	-90	-	dBc/Hz
		100 kHz Offset	-	-92	-	dBc/Hz
		1 MHz Offset	-	-122	-	dBc/Hz
	PLL Phase-Noise Performance@1620.1MHz PFD Frequency：10MHz Loop Bandwidth：60KHz	1kHz Offset	-	-83	-	dBc/Hz
		10 kHz Offset	-	-80	-	dBc/Hz
		100 kHz Offset	-	-93	-	dBc/Hz
		1 MHz Offset	-	-118	-	dBc/Hz
	PLL Phase-Noise Performance@3240.1MHz PFD Frequency：10MHz Loop Bandwidth：60KHz	1kHz Offset	-	-80	-	dBc/Hz
		10 kHz Offset	-	-79	-	dBc/Hz
		100 kHz Offset	-	-83	-	dBc/Hz
		1 MHz Offset	-	-114	-	dBc/Hz

ESD WARNING

	ESD (electrostatic discharge) sensitive devices. Charged devices and circuit boards can discharge without notice; high-energy ESD may damage the device. Always use appropriate ESD precautions to prevent performance degradation or loss of functionality.

Timing Characteristics (Unless otherwise specified, AVDD_BUFF = AVDD_DIV = AVDD_PFD = AVDD_PRE = AVDD_CP = AVDD_VCO2 = AVDD_VCO3 = AVDD_VCO4 = DVDD_DIG = 1.8V ±5%, AVDD_VCO1 = 2.5V ±5%, and DVDD_LST = 2.4V to 3.6V. The operating temperature is TA = -55°C to +125°C. The high-level potential is 2.5V to 3.3V, the low-level potential is 0V, the maximum clock frequency is Fmax = 25 MHz, and the period is T = 40 ns.)

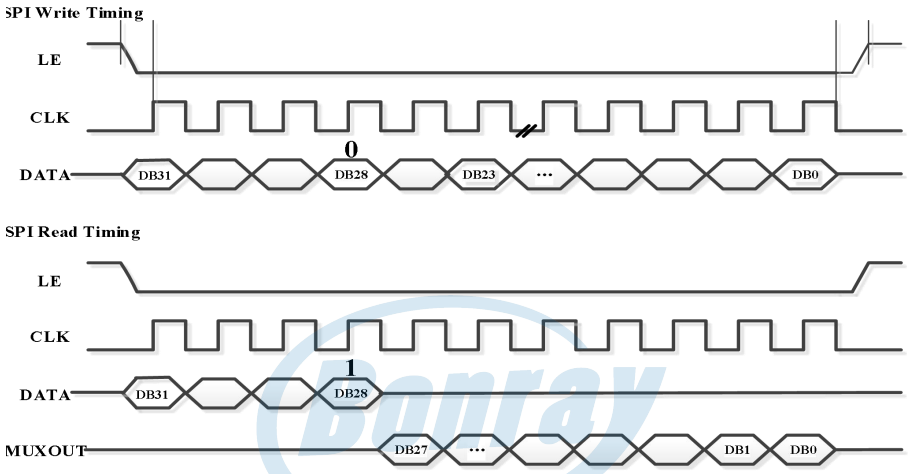


Figure 2. Timing Diagram of SPI Read/Write Operation Modes

Note: 1. Register REG0 must be configured last to refresh all register data.

2. First send the address bits, then the read/write bit, and finally the data bits. The higher bits of the address are sent first, and the higher bits of the data are sent first.

3. The host (master) sends data on the falling clock edge, while the slave receives data on the rising clock edge.

4. The maximum supported SPI clock rate is 25MHz.

5. A minimum interval of 10 clock edges is recommended between register configurations.

6. Ensure the reference signal input is normal before configuration.

Typical Performance

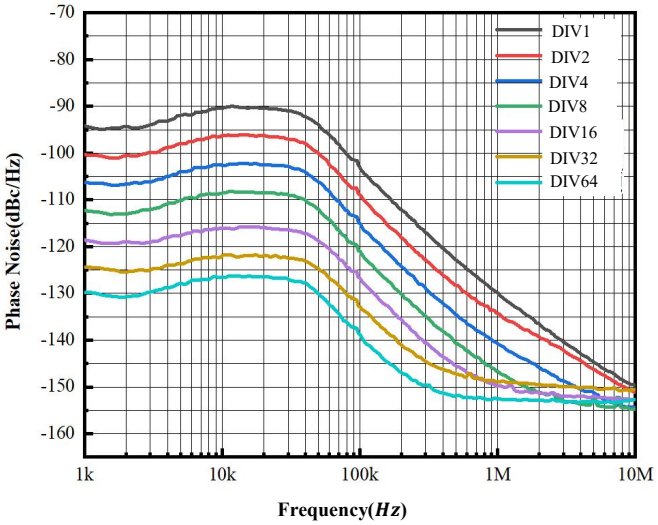


Figure3. 1.62GHzNoise Performance@60KHzLoop Bandwidth

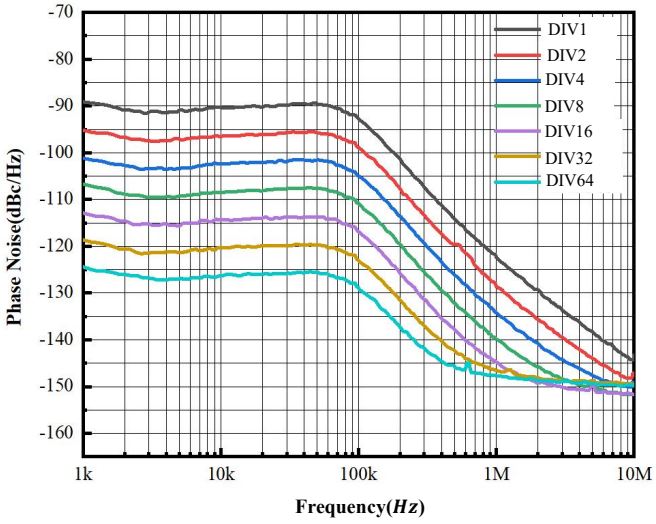


Figure4. 3.24GHzNoise Performance@60KHzLoop Bandwidth

Loop Bandwidth

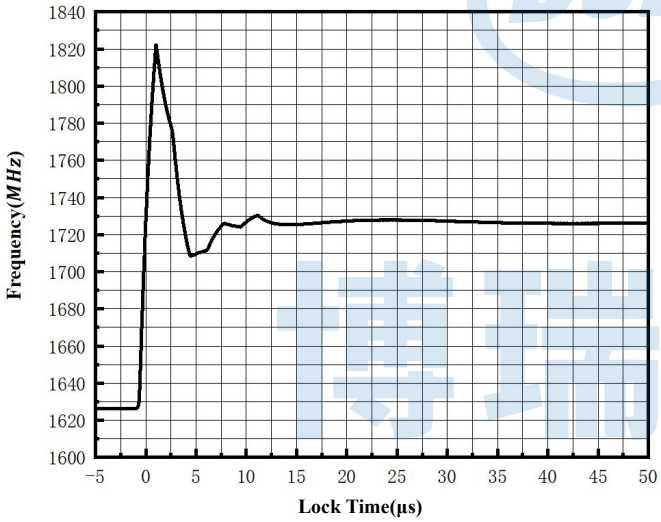


Figure5. 60KHzLoop Bandwidth stepping up100MHz Lock time

Loop Bandwidth

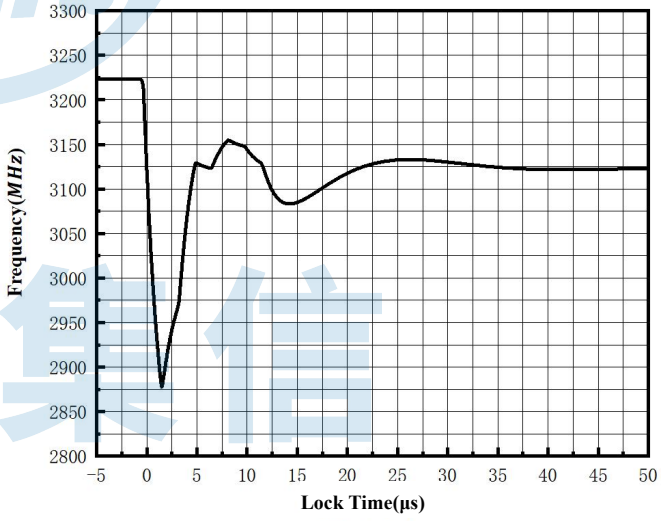


Figure6. 60KHzLoop Bandwidth stepping down100MHz Lock time

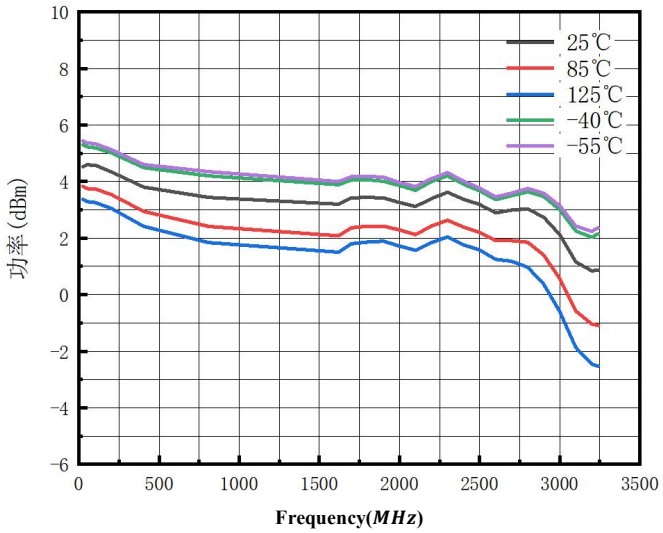


Figure7. RFOUT+/-output power

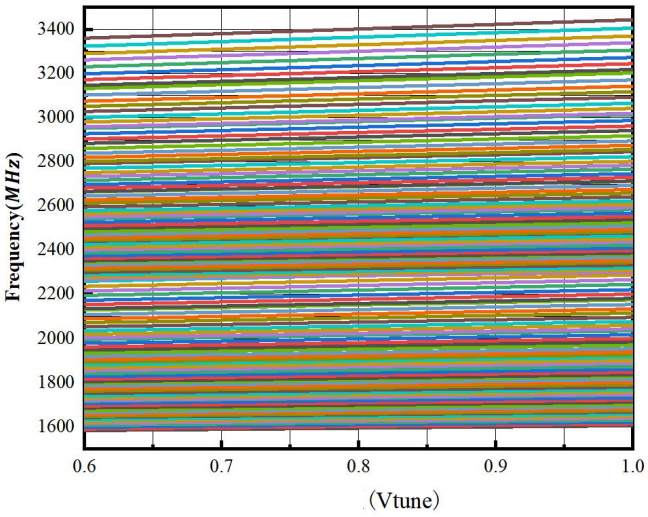
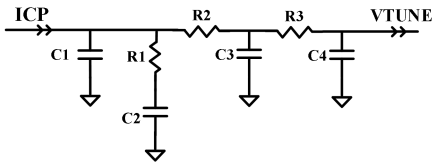


Figure8. VCO Output Frequency Tuning Curve

Table 3. Loop Filter Design Reference

Loop Filter Number	Loop Filter Bandwidth(KHz)	C1 (nF)	R1 (Ω)	C2 (nF)	R2 (Ω)	C3 (nF)	R3 (Ω)	C4 (nF)	Loop Filter Design Reference Diagram
1	40	4.7	130	87.6	82	3.1	470	1	
2（Recommend）	60	2.2	200	38.6	130	1.4	680	0.47	
3	80	1.2	270	22	160	0.78	910	0.252	

Note: It is recommended that the loop filter be designed with a phase detection frequency of 50MHz and an ICP current of 400uA. Both integer and fractional performance are better compared to a phase detection frequency of 20MHz.

Pin Function

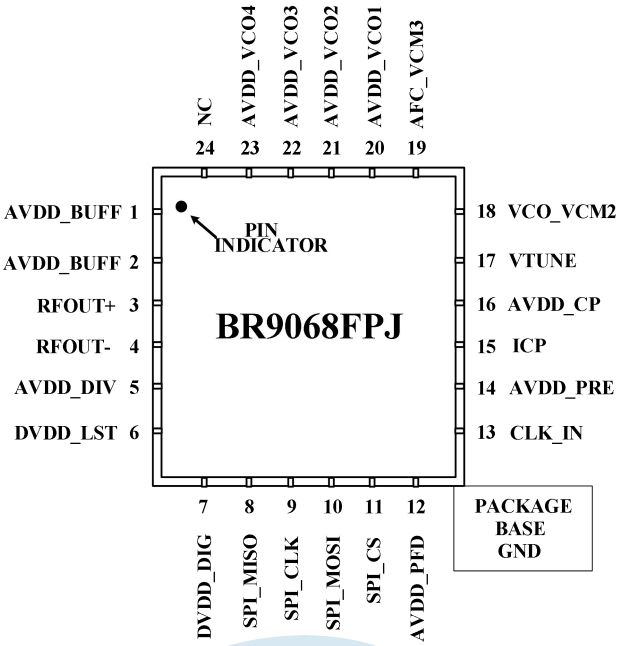


Figure 9 Pinout

Table 4. Description

Pin Number	Pin Name	Description
1	AVDD_BUFF	Analog power1.8V
2	AVDD_BUFF	Analog power1.8V
3	RFOUT+	Radio Frequency Output Port
4	RFOUT-	Complementary Radio Frequency Output Port
5	AVDD_DIV	Analog power1.8V
6	DVDD_LST	Digital power 2.5V
7	DVDD_DIG	Digital power 1.8V
8	SPI_MISO	Multiplexer output, which can access lock detection, prescaled reference clock, N-divided feedback clock, and SPI read mode
9	SPI_CLK	Serial communication data line (chip input)
10	SPI_MOSI	Serial communication clock line
11	SPI_CS	Serial communication chip select line
12	AVDD_PFD	Analog power1.8V
13	CLK_IN	Reference clock input. An external DC-blocking capacitor is required.
14	AVDD_PRE	Analog power1.8V
15	ICP	Charge pump output. This pin provides ±Icp to the external loop filter and is connected to the ICP port of the external loop filter.
16	AVDD_CP	Analog power1.8V

17	VTUNE	VCO control voltage, externally connected to the VTUNE port of the loop filter output
18	VCO_VCM2	Internal bias port, externally connected to a 4.7uF grounded decoupling capacitor. 0.53V
19	AFC_VCM3	Internal bias port, externally connected to a 4.7uF grounded decoupling capacitor. 0.8V
20	AVDD_VCO1	Analog power，2.5V， externally connected to a20uF。
21	AVDD_VCO2	Analog power1.8V
22	AVDD_VCO3	Analog power1.8V
23	AVDD_VCO4	Analog power1.8V
24	NC	No Connect

Register Description

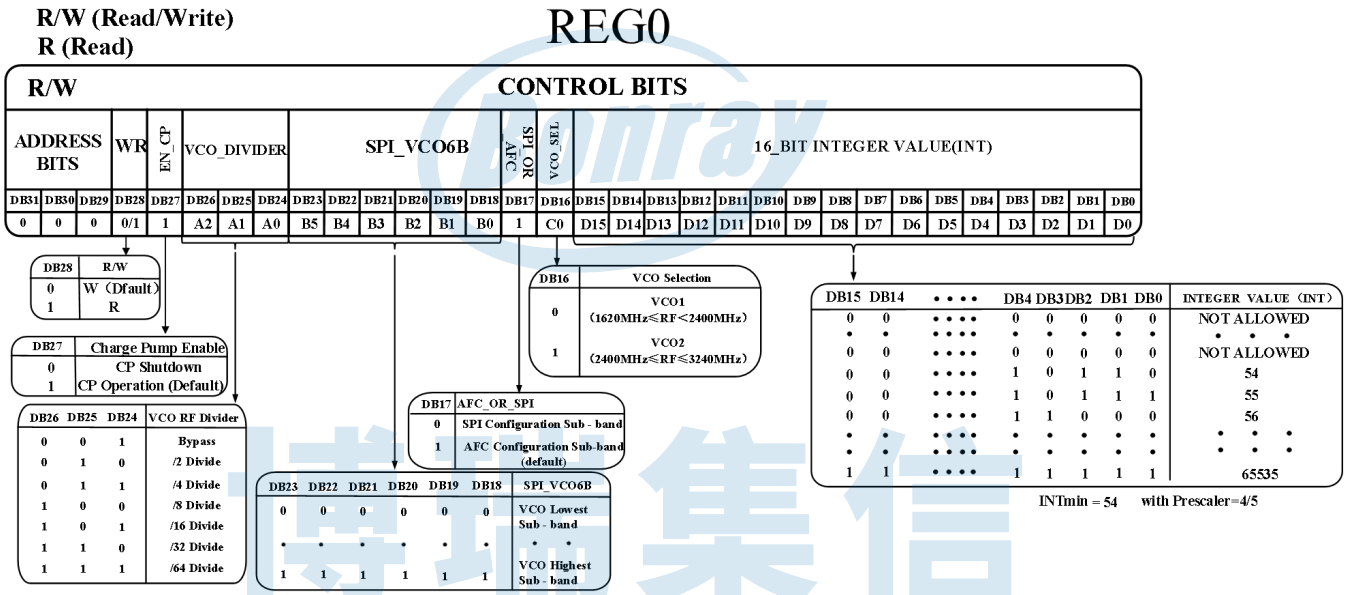


Figure 10 Configuration Information of reg0 Register

REG1

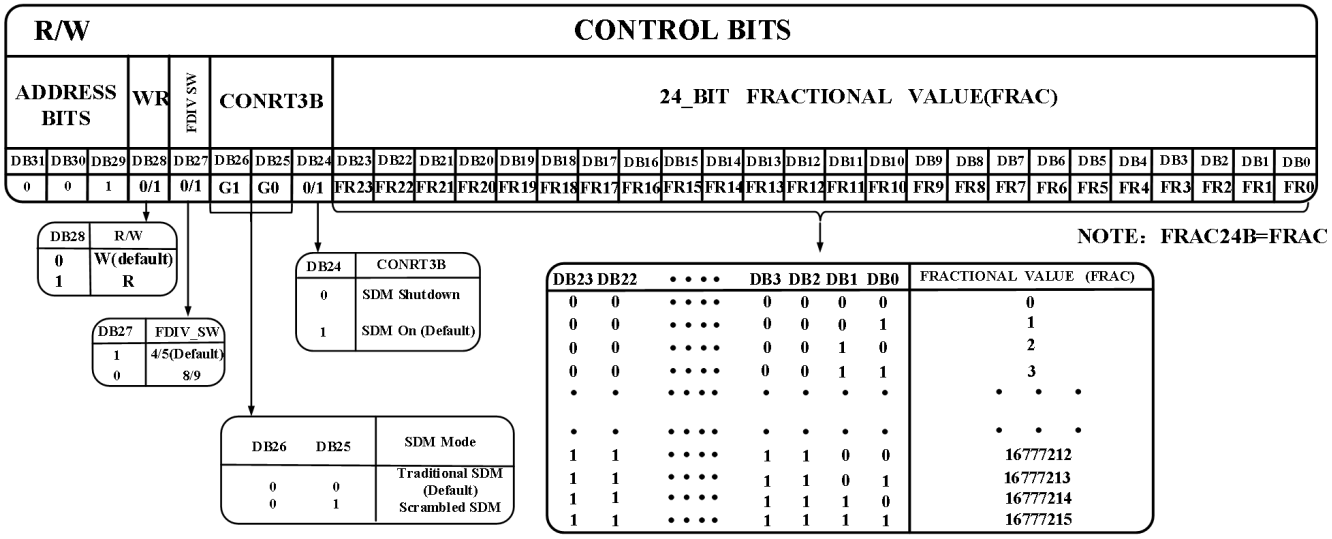


Figure 11 Configuration Information of reg1 Register

REG2

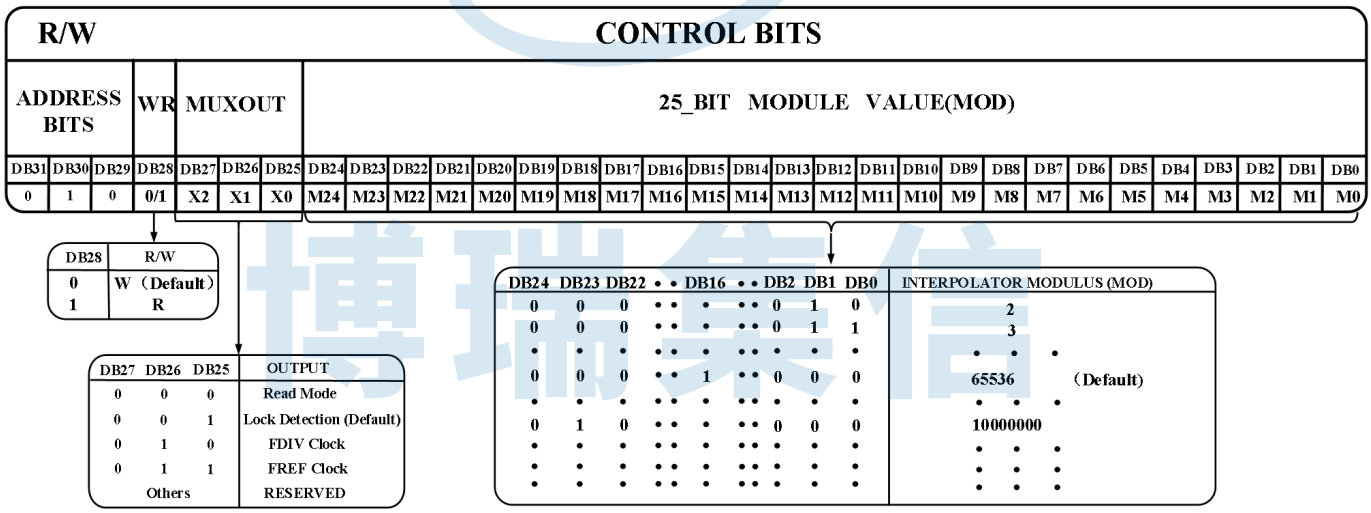


Figure 12 Configuration Information of reg2 Register

REG3

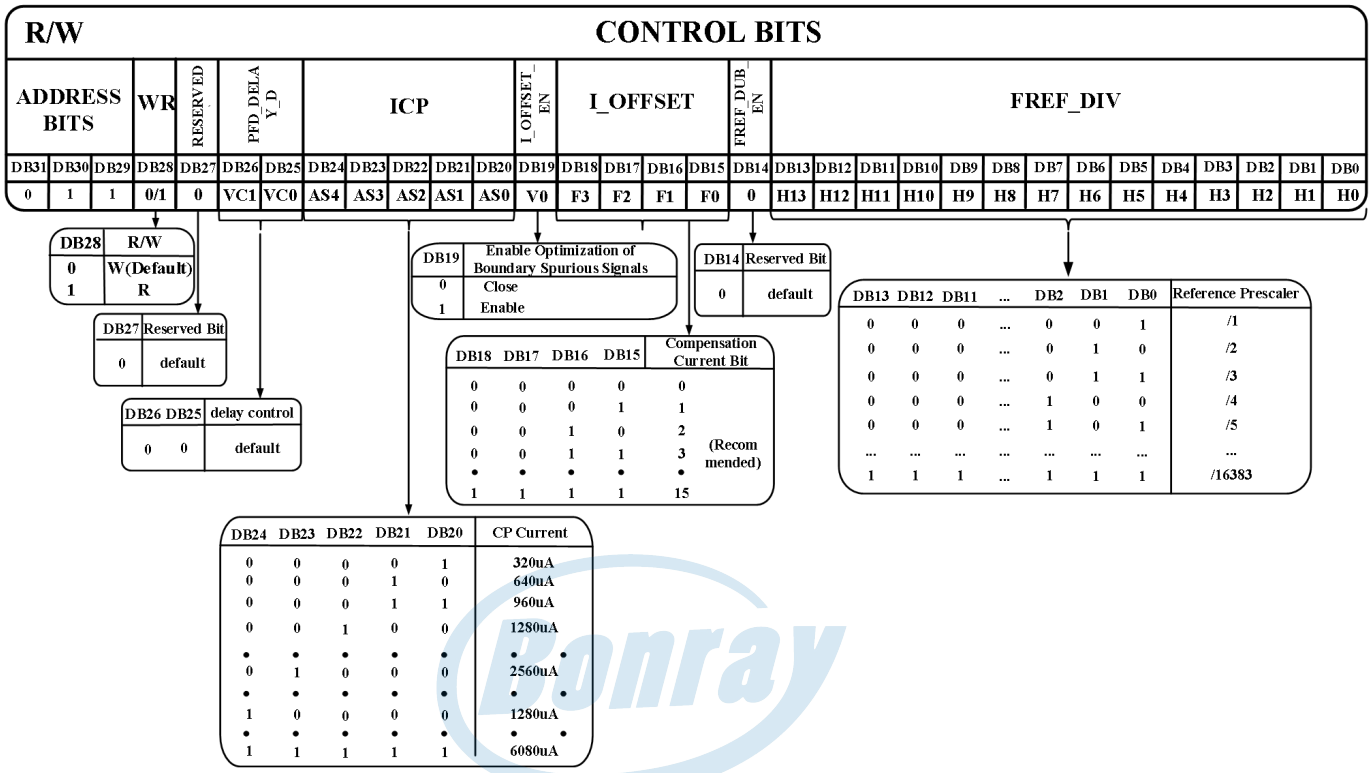


Figure 13 Configuration Information of reg3 Register

REG4

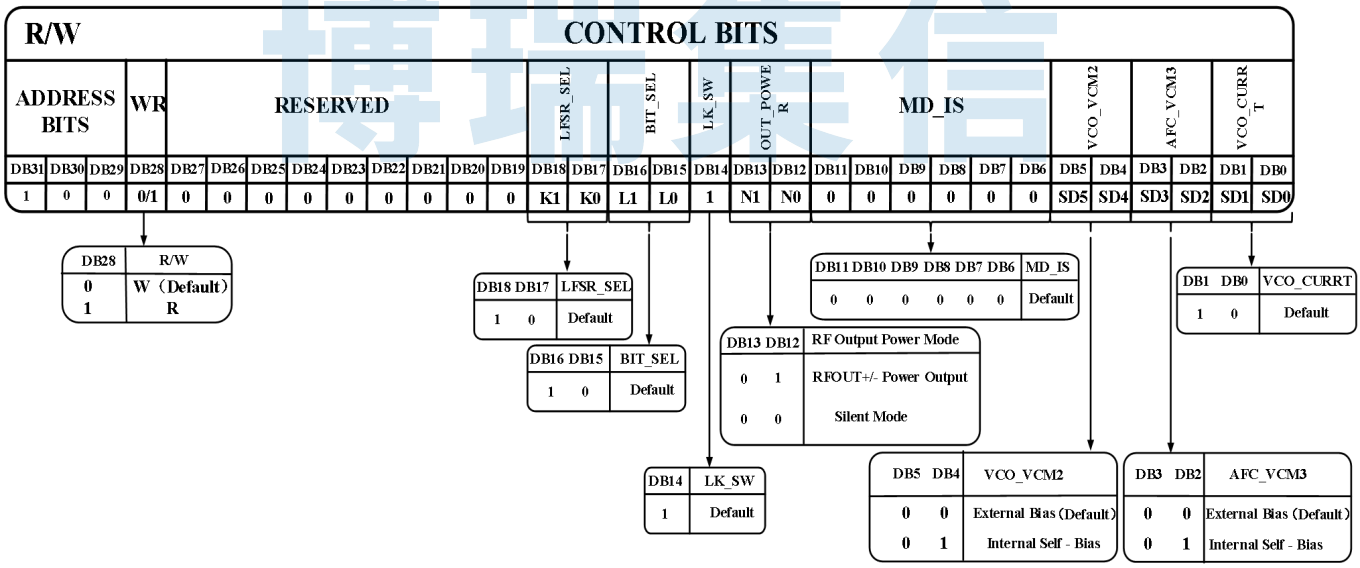


Figure 14 Configuration Information of reg4 Register

Register 0

Address Bits

When the address bits DB[31:29] of Register 0 = 3'b000, Register 0 can be programmed.

Read/Write Bit

When the read/write bit DB[28] of Register 0 = 1'b0, write operations can be performed on Register 0.

Charge Pump Enable Bit

The charge pump enable bit DB[27] of Register 0 is used to control the charge pump current switch. The default setting is charge pump current ON (DB[27] = 1'b1).

VCO RF Divider Setting Bits

The VCO RF divider setting bits DB[26:24] of Register 0 are used to divide the RF output frequency by 1 to 64, enabling the expansion of the frequency range. For specific configurations, refer to the reg0 register configuration information.

VCO Sub-band 6-bit Control Bits

The VCO sub-band 6-bit control bits DB[23:18] of Register 0 are used to select among 64 different VCO sub-bands. This function must be used in conjunction with the SPI_OR_AFC selection setting bit (control bit DB[17]).

SPI or AFC Selection Setting Bit

The SPI or AFC selection setting bit DB[17] of Register 0 is used to choose between automatic VCO sub-band selection or SPI-configured sub-band selection. When DB[17] = 1'b1, the AFC (Automatic Frequency Calibration) function automatically selects the VCO sub-band corresponding to the target RF output frequency.

When DB[17] = 1'b0, the VCO sub-band corresponding to the target RF output frequency is manually configured via SPI. This function must be used in conjunction with the VCO sub-band 6-bit control bits.

VCO Selection Setting Bit

The VCO selection setting bit DB[16] of Register 0 is used to select the VCO for different RF frequency band outputs. When 1620 MHz ≤ RF output frequency < 2400 MHz, select the low-band VCO. When 2400 MHz ≤ RF output frequency ≤ 3240 MHz, select the high-band VCO.

INT Value Setting Bits

The INT value setting bits DB[15:0] of Register 0 are used to set the INT value, which determines the integer part of the feedback division factor. It is used in the formula:

$RF_{OUT} = [INT + (FRAC/MOD)] \times [f_{PFD}]/RF$分频器。

WhereRF_{OUT}s the RF output frequency, INT is the integer part of the feedback division factor,，$INT$is the integer part of the feedback division factor，$FRAC/MOD$is the fractional part of the feedback division factor，$f_{PFD}$is the PFD frequency, and the RF divider is the VCO RF divider (1~64 division).

Register 1

Address Bits

When the address bits DB[31:29] of Register 1 = 3'b001, Register 1 can be programmed.

Read/Write Bit

When the read/write bit DB[28] of Register 1 = 1'b0, write operations can be performed on Register 1.

Dual-Modulus Prescaler Setting Bit

The dual-modulus prescaler setting bit DB[27] of Register 1 is used to set 4/5 division or 8/9 division. Since the maximum RF frequency allowed by the dual-modulus prescaler using synchronous 4/5 division meets the highest frequency requirement, the full-band setting for BR9068FPJ defaults to 4/5 division.

SDM Mode and Switch Setting Bits

The SDM mode and switch setting bits DB[26:24] of Register 1 are used to set the SDM mode and switch. When the SDM mode and switch DB[26:24] = 3'b001, the SDM operates in legacy mode, which achieves lower phase noise performance but with larger fractional spurs. When the SDM mode and switch DB[26:24] = 3'b101, the SDM operates in dither mode, which optimizes fractional spurs, while phase noise performance degrades.

FRAC Setting Bits

The FRAC setting bits DB[23:0] of Register 1 are used to set the numerator value for the Sigma-Delta Modulator (SDM) fractional input. They are used in conjunction with the denominator MOD value to implement the fractional part of the feedback division factor.

Register 2

Address Bits

When the address bits DB[31:29] of Register 2 = 3'b010, Register 2 can be programmed.

Read/Write Bit

When the read/write bit DB[28] of Register 2 = 1'b0, write operations can be performed on Register 2.

MUXOUT Setting Bits

The MUXOUT setting bits DB[27:25] of Register 2 are used to access functions such as lock detection, the reference clock after prescaling, the feedback clock after N-division, and SPI read, etc. The default is to access lock detection.

MOD Modulus Setting Bits

The MOD modulus setting bits DB[24:0] of Register 2 are used to set the denominator modulus value for the SDM fractional input. They are used in conjunction with the numerator FRAC value to implement the fractional part of the feedback division factor. The default MOD modulus setting is DB[24:0] = 25'd65536 (a 25-bit value 65536).

Register 3

Address Bits

When the address bits DB[31:29] of Register 3 = 3'b011, Register 3 can be programmed.

Read/Write Bit

When the read/write bit DB[28] of Register 3 = 1'b0, write operations can be performed on Register 3.

Charge Pump Current Setting Bits

The charge pump current setting bits DB[24:20] of Register 3 are used to set the charge pump current. The minimum charge pump current is 320 μA, with a step size of 320 μA, and the maximum achievable current is 6.08 mA. The loop bandwidth can be modified by appropriately adjusting the ICP current, trading off performance between integer and fractional frequency points.

OFFSET Current Enable Bit

The OFFSET current enable bit DB[19] of Register 3 is used to optimize spurs at integer boundaries. When fractional boundary spurs fall in-band and are difficult to suppress via the loop bandwidth, setting DB[19] = 1'b1 can optimize these boundary spurs. However, this introduces current noise, degrading phase noise performance and reference spur performance.

eference Prescaler Setting Bits

The reference prescaler setting bits DB[13:0] of Register 3 are used to divide the input reference clock frequency (REFIN) to meet the input frequency range requirements of the phase detector.

Register 4

Address Bits

When the address bits DB[31:29] of Register 4 = 3'b100, Register 4 can be programmed.

BitsRead/Write Bit

When the read/write bit DB[28] of Register 4 = 1'b0, write operations can be performed on Register 4.

RFOUT+/- RF Output Power Mode Setting RFOUT+/-

The RFOUT+/- RF output power mode setting bits DB[13:12] of Register 4 are used to control the output and mute states of the RFOUT+/- RF power. When DB[13:12] = 01, it is in RF power output mode. When DB[13:12] = 00, it is in RF output mute mode, where the power of the mute output lock signal is ≤ -52dBm.

Register 0~5 Configuration Sequence

After sequentially placing 1uF, 0.1uF, and 0.01uF capacitors at the power supply pin connections to maximally filter out interference on the power lines and ensure proper power-up, configure the BR9068FPJ in the following register order:

Frequency Point Configuration Instructions

The following is an application example illustrating how to configure the BR9068FPJ:

RF_{OUT}=[INT+(FRAC/MOD)]×[f_{PFD}]/RF divider

Among them, RF_{OUT} is the RF output frequency, INT is the integer division coefficient, FRAC is the fractional division coefficient, MOD is the modulus, f_{PFD} is the phase detector frequency, and the RF divider is the RF output division number of the VCO.

f_{PFD} = REFIN × [1/R] where REFIN is the reference frequency input and R is the reference prescaling coefficient.

Suppose the existing RF system needs an output frequency (RF_{OUT}) of 3000.2MHz, the frequency of the reference crystal oscillator (REFIN) is 20MHz, and the frequency channel resolution (f_{RESOUT}) is 200KHz. Thus:

The VCO output frequency of BR9069FLJ is 3000 - 6000MHz, so the RF divider = 1; the output requirement of the RF divider is a 200KHz channel resolution (f_{RESOUT}), so the channel resolution of the VCO output is also 200KHz (f_{RES}).

MOD =65536

f_{PFD} = 20MHz × [(1)/(1)]=20MHz

$3000.2=20\times [INT + \left(\frac{FRAC}{65536}\right)]$

It can be obtained that: INT =150

FRAC=655

In the above calculation, the MOD value is 65536. And when calculating f_{PFD}, the reference division factor R is set to 1. The value of f_{PFD} here can be flexibly set, but it should be less than or equal to the maximum phase - detection frequency of the PFD.。

Application Information

Figure 15 shows the typical application circuit of BR9069FLJ. The chip is powered by 3.3V and 1.2V power supplies, and it is recommended to use an LDO for chip power supply. The noise performance of the LDO will reduce its impact on the noise performance of BR9069FLJ. The chip requires an external loop filter to work, and a 4th-order loop filter is recommended. The input reference signal needs to be provided by an external crystal oscillator.

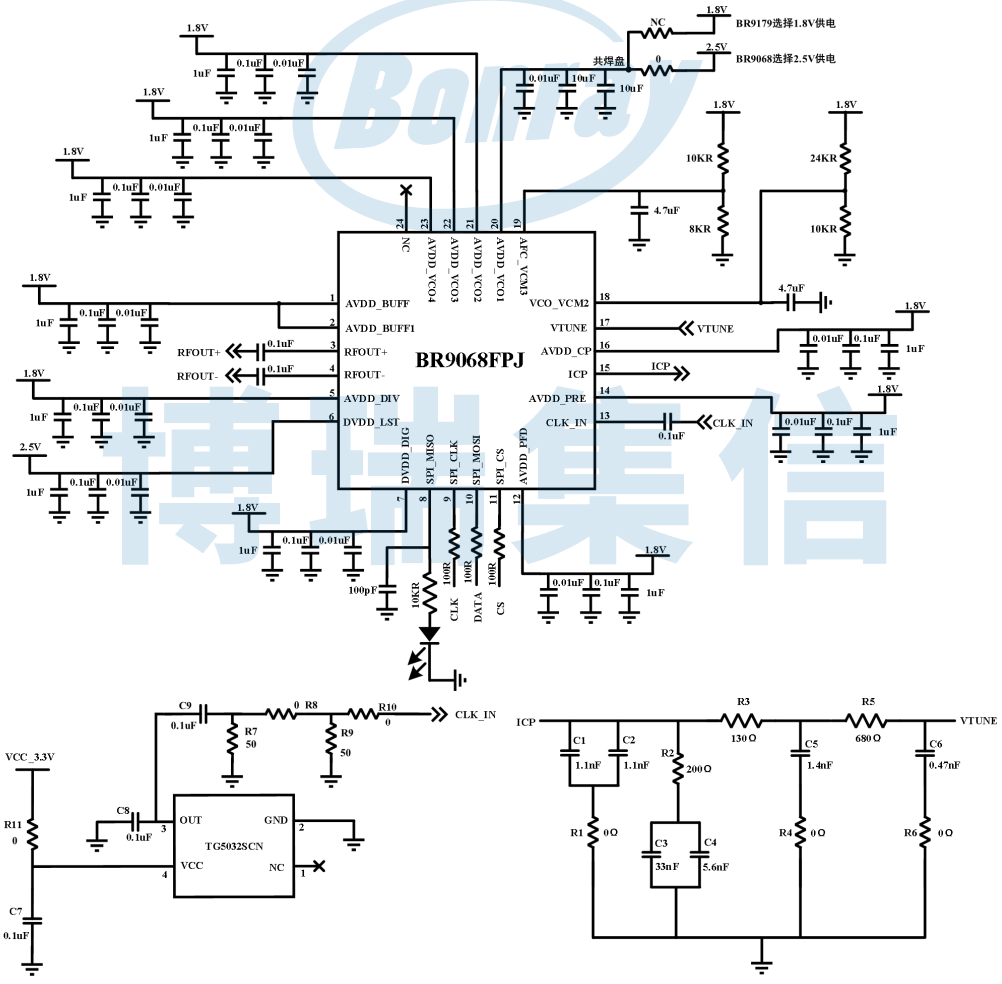
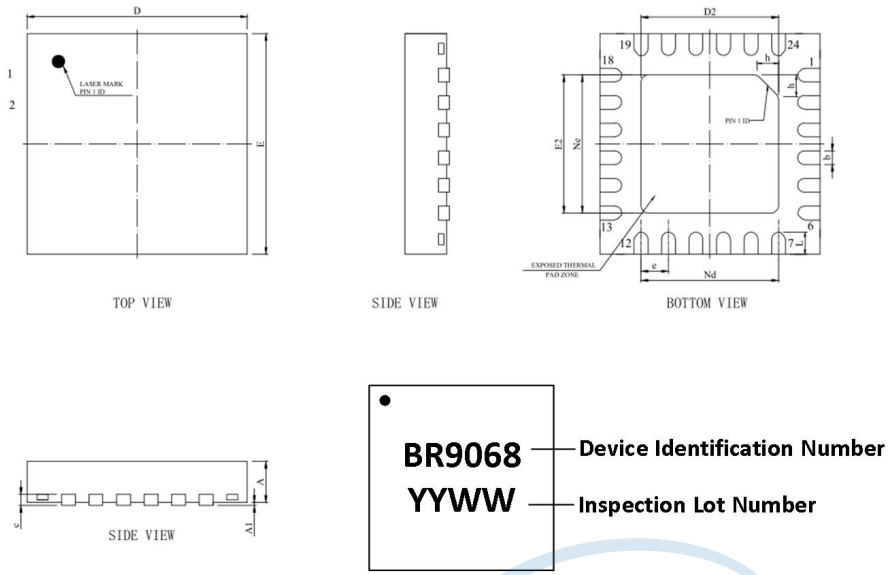


Figure 15 Typical Application Circuit

Package Information (Unit: mm)



SYMBOL 符 号	MILLIMETER 毫 米		
	MIN 最小	NOM 标称	MAX 最大
A	0.75	0.80	0.85
A1	0.01	0.02	0.05
b	0.20	0.25	0.30
c		0.270REF	
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
L	0.35	0.40	0.45
h	0.35	0.40	0.45

Figure 16 Package Information Diagram