Product Features

Frequency: 13.75GHz ~ 15.5GHz

S21: 21.5dB@14.5GHz

OP1: 31dBm@14.5GHz

Psat: 32.0dBm@14.5GHz

PAE: 34%@14.5GHz

V_{DD}=+8V with I_{DQ} 350mA

Package: QFN24 (4mmx4mm)

Applications

Satcom

Radar

General Description

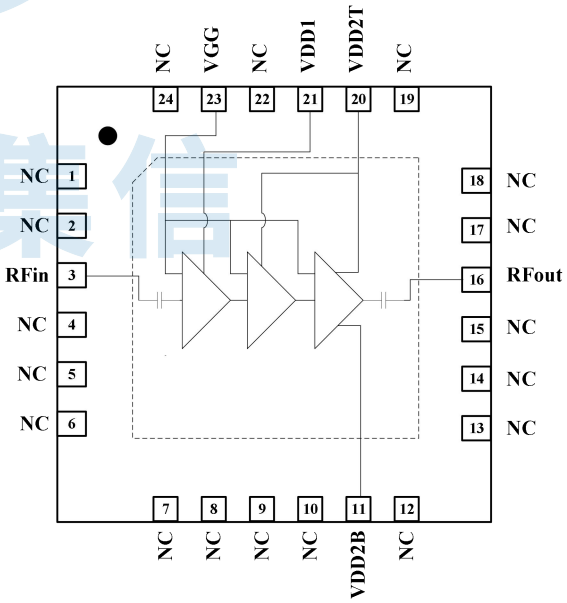
The BR9773FPJ is a high out-of-band rejection, internally matched MMIC driver amplifier. It delivers 21.5dB small-signal gain and achieves an OP1dB of 31dBm at 14.5 GHz. The amplifier is perfectly suited for transmitter systems in satellite and microwave scattering communications.

The BR9773FPJ is housed in a QFN24 SMT package and operates from a +8V drain supply with a quiescent current of 350mA.

Ordering Information

Part Number	Package	Description
BR9773FPJ	QFN24	13.75GHz~15.5GHz Driver Amplifier

Functional Block Diagram



Electrical Specifications: EVB test data (13.75GHz~15.5GHz)

Parameters	Test Condition	Min	Typ.	Max	Units
Gain	13.75GHz	—	23.0	—	dB
	14.5GHz	—	21.5	—	dB
	15.5GHz	—	21.5	—	dB
Input Return Loss	13.75GHz	—	12	—	dB
	14.5GHz	—	13.6	—	dB
	15.5GHz	—	17.1	—	dB
Output Return Loss	13.75GHz	—	18.5	—	dB
	14.5GHz	—	20.4	—	dB
	15.5GHz	—	14.0	—	dB
Isolation	13.75GHz	—	57.1	—	dB
	14.5GHz	—	57.3	—	dB
	15.5GHz	—	60.0	—	dB
OP1	13.75GHz	—	30.8	—	dBm
	14.5GHz	—	31.2	—	dBm
	15.5GHz	—	30.7	—	dBm
PAE@P_{sat}	13.75GHz	—	30.5	—	%
	14.5GHz	—	34.3	—	%
	15.5GHz	—	30.6	—	%
Supply Voltage	—	—	8	9	V
Quiescent Current	—	—	350	—	mA
Test Condition: V_{DD}=+8V, V_{GG}=-0.8V, TA=+25℃					

Absolute Maximum Ratings

Maximum Operating Voltage: +9V

Maximum RF Input Power: +24dBm

Recommended Operating Conditions Voltage (V_{DD}): +8V (Typ)

Gate Voltage (V_{GG}): -0.8V (Typ)

Quiescent Drain Current (I_{DQ}): 350mA (Typ)

Storage Temperature: -65℃~+150℃

Operating Temperature: -55℃~+125℃

Note: Absolute Maximum Ratings define the limiting values that the device can withstand. Exceeding these ratings may cause permanent damage to the device. Prolonged operation under absolute maximum rating conditions may impair device reliability.

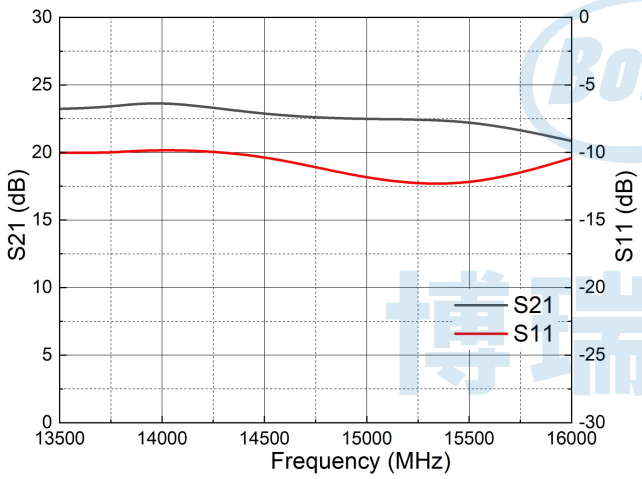
ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

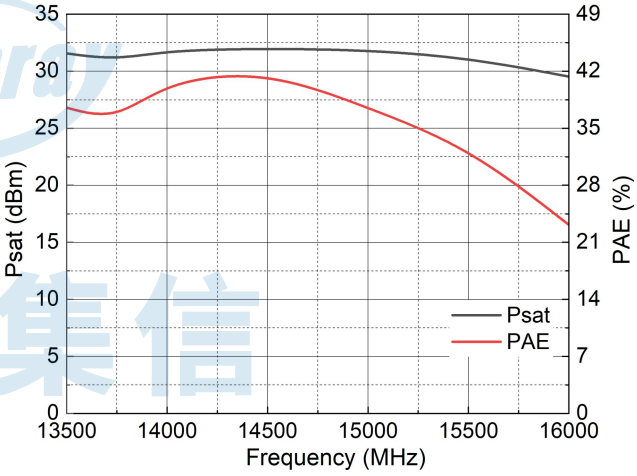
OBSERVE HANDLING PRECAUTIONS

Typical Performance: (EVB test data, 13.75GHz~15.5GHz)

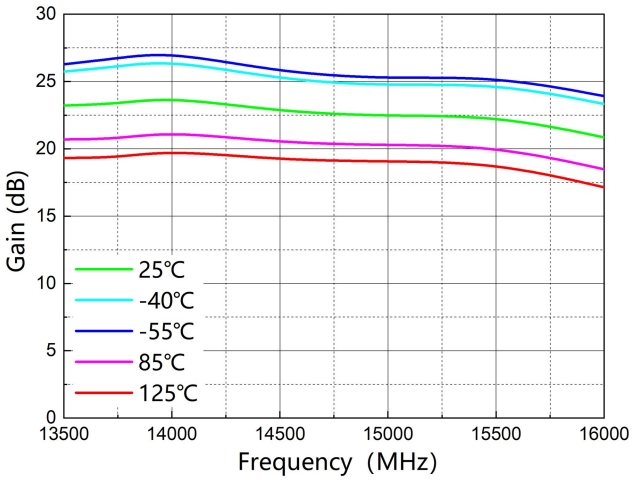
Parameters	Typ.						Units
Frequency	**13.5**	**13.75**	**14**	**14.5**	**15**	**15.5**	**GHz**
Gain	22.7	23.1	22.8	21.5	21.5	21.5	dB
Input Return Loss	12.2	12.0	12.2	13.6	17.5	17.2	dB
Output Return Loss	16.7	18.5	18.7	20.4	16.7	14.0	dB
Isolation	59.8	57.2	56.3	57.1	58.0	60.3	dB
OP1&Psat	30.8	30.8	31.0	31.2	31.3	30.7	dBm
I_C@P_{sat}&OP1	487	486	461	474	479	476	mA
PAE@P_{sat}	30.3	30.5	33.8	34.4	34.3	30.6	%
Test Condition: Temp=+25℃, V_{DD}=+8V, V_{GG}=-0.8V, I_{DQ}=350mA							



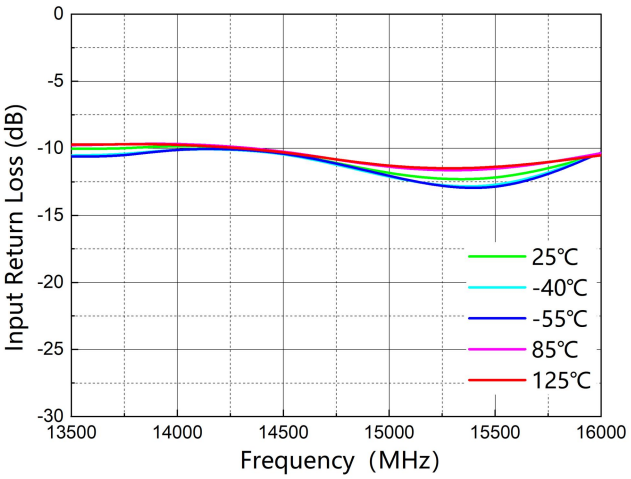
Gain, Input Return Loss vs. Freq



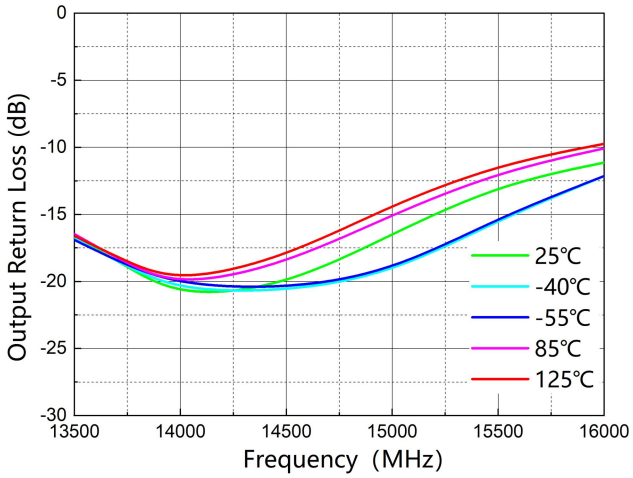
Psat, PAE vs. Freq



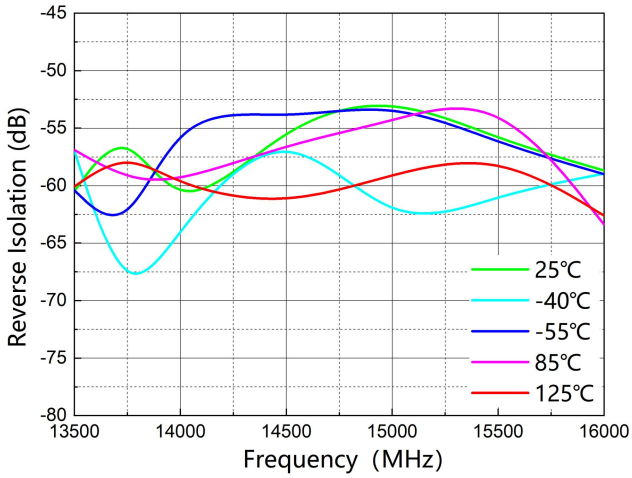
Gain vs. Freq



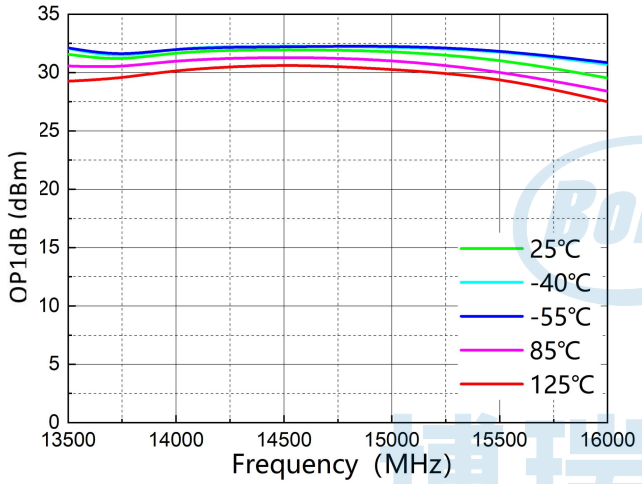
Input Return Loss vs. Freq



Output Return Loss vs. Freq

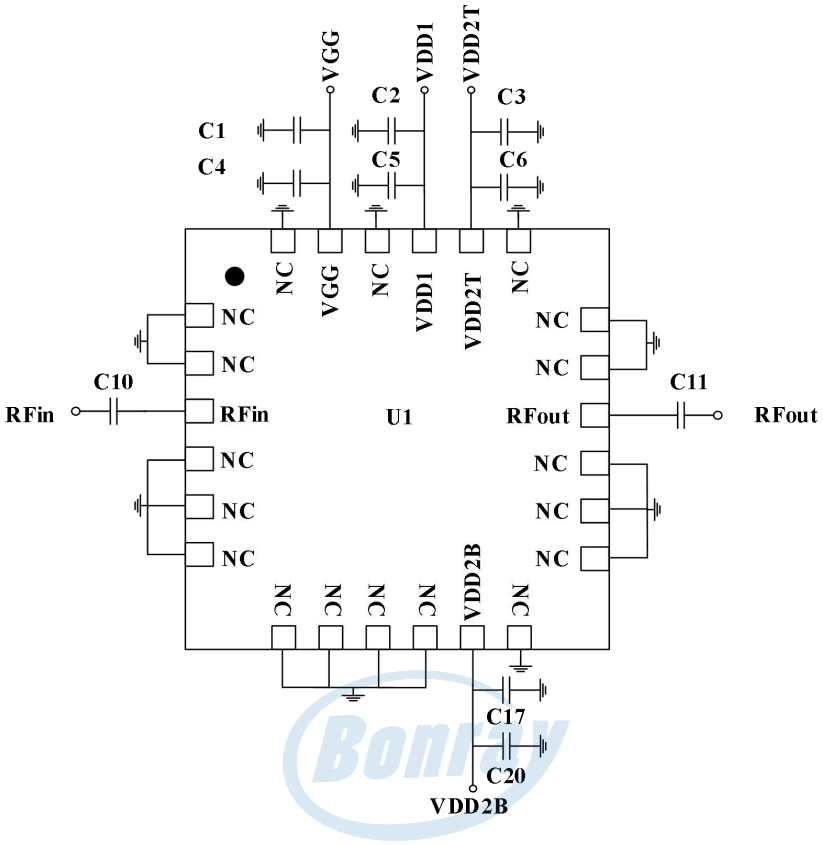


Reverse Isolation vs. Freq



OP1dB vs. Freq

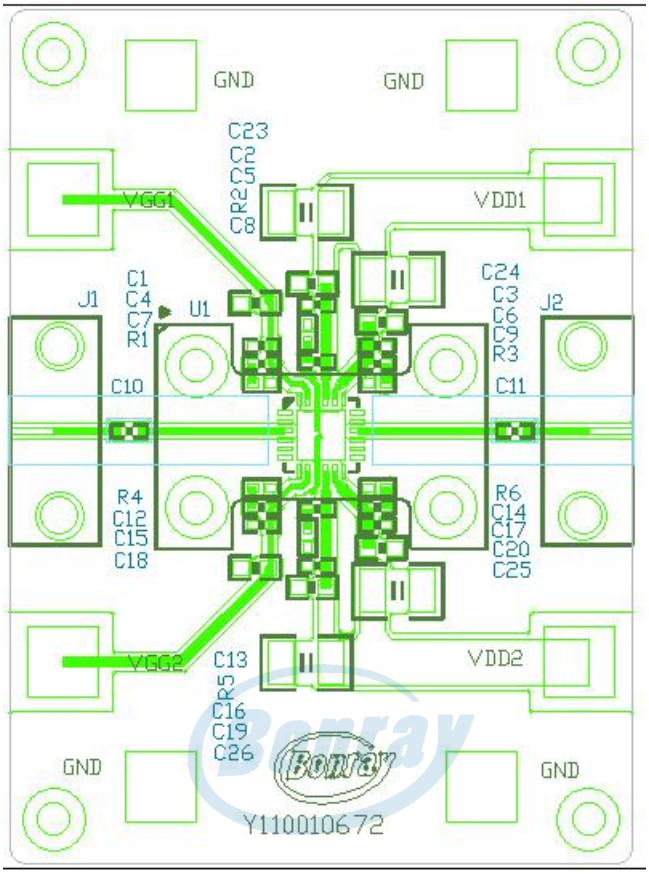
Application Information



Bill of Material

Designator	Package	Value	Part Number
C1、C2、C3、C20	C0603	4.7uF	GRM188C71C475KE21D
C4、C5、C6、C10、C11、C17	C0402	1nF	GRM1555C1H102JA01D

Evaluation Board (10mil Rogers 4350B PCB)



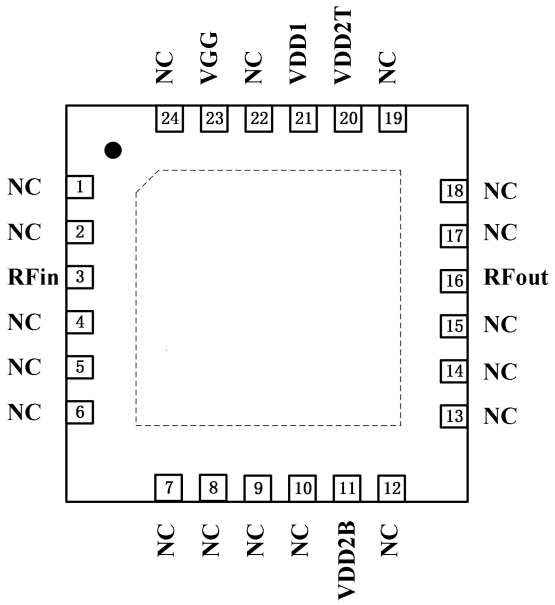
PCB Layout Guidelines

1、The backside pad of the chip is used for RF grounding and heat dissipation. It is recommended to place as many ground vias as possible in the corresponding area (e.g., with a via diameter of 0.3mm, the number of ground vias should be no less than 25, as shown in the figure above).

2、To ensure proper heat dissipation and grounding performance, it is recommended to connect the bottom side of the PCB to the external heat dissipation structure using thermal grease.

3、Ensure that screws are installed around the chip to securely fasten it to the mechanical structure.

Pin layout and Description



Pin Description

Pin Number	Pin Name	Description
1-2、4-10、12-15、17-19、22、24	NC	Internally not connected, recommended to be grounded in application.
3	RFin	This pin is the RF input, internally matched to 50Ω.
16	RFout	This pin is the RF output, internally matched to 50Ω.
23	VGG	Gate voltage.
21、20、11	VDD1、VDD2T、VDD2B	Drain voltage.
/	Backside	DC and RF Ground

Power-on Sequence

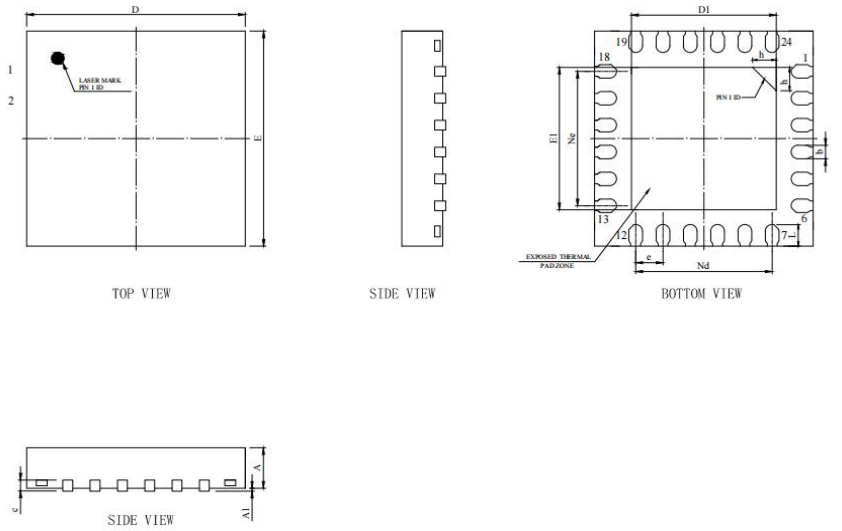
1. Set the grid voltage (VGG) to -3V,Turn on the gate voltage
2. Set drain voltage (VDD) to +8V,Turn on the drain voltage
3. Adjust the gate voltage (Vgg) to set the drain current to 350 mA.
4. Input RF signal.

Power-off Sequence

1. Turn off the RF signal
2. Turn off the drain votage and wait for 5 seconds to allow the drain capacitors to fully discharge.
3. Turn off the gate voltage.

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that VGG is fully powered up before VDD is applied, and that VDD is lowered to below 1V before VGG is powered down, especially in TDD applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.80	0.90
A1	-	0.02	0.05
b	0.20	0.25	0.30
e		0.203REF	
D	3.90	4.00	4.10
D1	2.60	2.70	2.80
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E1	2.60	2.70	2.80
L	0.35	0.40	0.45
h	0.30	0.40	0.45

Package Outline Drawing

Recommended Soldering Temperature Profile