Product Features

Frequency Range: 3.5GHz ~ 4.5GHz

Phase Shift Range: 360°, LSB=5.625°

Insertion Loss: 4.6dB@4GHz

Input Return Loss: 14.2dB@4GHz

RMS Phase Error: 1.4°

Supply Voltage: -5V

Control Voltage: 0/+5V

Package: QFN24（4mm*4mm）

Apply

Communication Base Station

Data Link

Radar

Phased Array

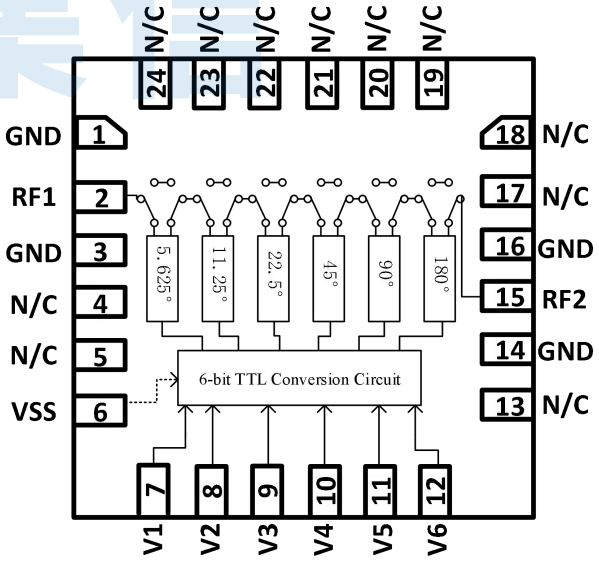
Ordering Information

Part Number	Package	Description
BR9597FPJ	QFN24	3.5GHz ~ 4.5GHz 6-Bit Parallel Digital-Controlled Phase Shifter

General Description

The BR9597FPJ is a 6-Bit Parallel Digital-Controlled Phase Shifter chip covering a frequency range of 3.5 GHz to 4.5 GHz. It features 0V/+5V logic control and requires an external-5V supply for bias. providing 360 degrees of phase coverage, with a LSB of 5.625 degrees. It features a typical RMS phase error of 1.4 and a typical insertion loss of 4.6 dB. Packaged in a QFN24, it is suitable for a wide range of applications including communication base stations, Radar, and Phased Array systems.

Functional Block Diagram



Electrical Specifications (Temp=+25℃)

Parameters	Test condition	Min.	Typ.	Max.	Units
Insertion Loss (Reference State)	3500MHz	-	-4.3	-	dB
	4000MHz	-	-4.6	-	
	4500MHz	-	-4.5	-	
Input Return Loss (Reference State)	3500MHz	-	-12.0	-	dB
	4000MHz	-	-14.2	-	
	4500MHz	-	-20.4	-	
Output Return Loss (Reference State)	3500MHz	-	-14.8	-	dB
	4000MHz	-	-21.7	-	
	4500MHz	-	-24.1	-	
Phase Shift Amplitude Modulation	3500MHz	-0.09	-	0.56	dB
	4000MHz	-0.04	-	0.38	
	4500MHz	-0.38	-	0.24	
RMS Phase Error	3500MHz	-	1.38	-	°
	4000MHz	-	1.42	-	
	4500MHz	-	1.81	-	
Input Power for 1dB Compression (Reference State)	3500MHz	-	29.5	-	dBm
	4000MHz	-	29.8	-	
	4500MHz	-	29.7	-	

Absolute Maximum Ratings

Maximum RF Input Power: +30dBm

Maximum Supply Voltage: -5.5V

Recommended Operating Conditions

Control Voltage Threshold: 0~0.2V（“0”level）

2.7V~5V（“1”level）

Control Current: 1.1mA@5V

Storage Temperature: -65℃～+150℃

Operating Temperature: -55℃～+125℃

Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and exposure to absolute-maximum-ratings conditions for extended periods will affect the reliability.

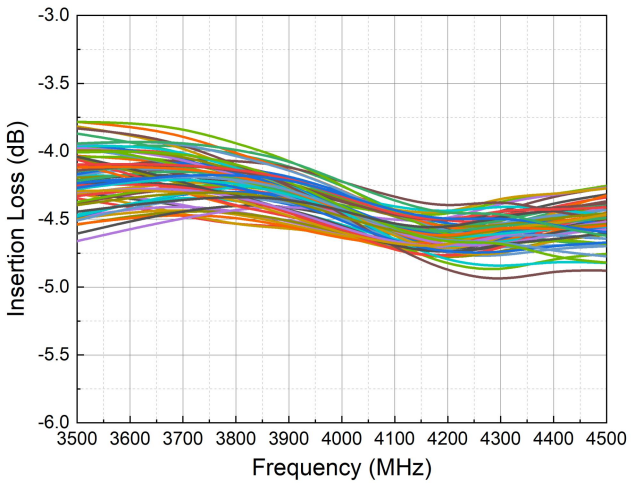
ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

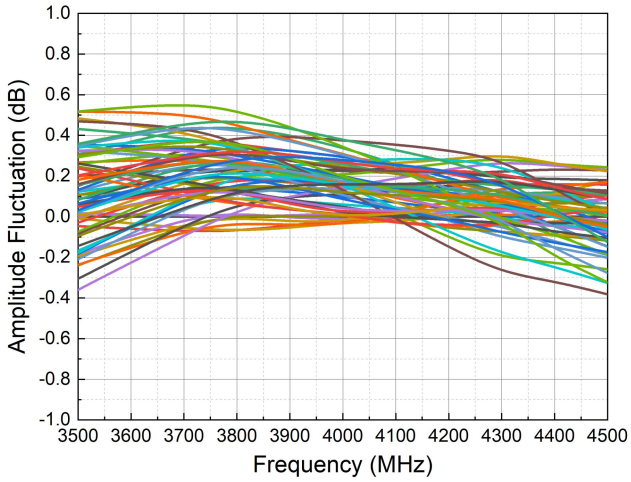
OBSERVE HANDLING PRECAUTIONS

Typical Performance (Temp=+25℃，EVB Test Results)

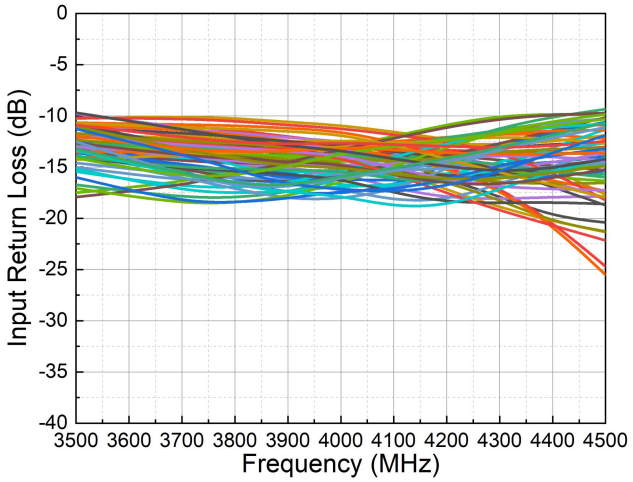
Parameters	Typ.										Units
Frequency	**3500**	**3700**	**3800**	**3900**	**4000**	**4100**	**4200**	**4300**	**4400**	**4500**	**MHz**
Phase Error (5.625°)	-0.16	0..07	0.24	0.33	0.31	0.30	0.21	0.27	0.32	0.17	°
Phase Error (11.25°)	-0.28	-1.10	-1.42	-1.60	-1.64	-1.60	-1.49	-1.32	-1.15	-0.92	°
Phase Error (22.5°)	-2.05	-2.15	-2.07	-1.94	-1.83	-1.73	-1.61	-1.42	-1.28	-1.24	°
Phase Error (45°)	1.18	0.46	0.16	0.09	0.14	0.24	0.49	0.87	1.32	1.75	°
Phase Error (90°)	2.32	1.37	0.75	0.49	0.55	0.77	0.96	0.97	1.20	1.45	°
Phase Error (180°)	-1.26	0.14	0.52	0.72	0.83	0.88	0.79	0.48	0.01	-0.62	°
Insertion Loss (Reference State)	-4.3	-4.4	-4.5	-4.5	-4.6	-4.7	-4.7	-4.6	-4.6	-4.5	dB
Input Return Loss (Reference State)	-12.0	-12.6	-13.1	-13.8	-14.2	-15.1	-16.1	-17.8	-19.8	-20.4	dB
Output Return Loss (Reference State)	-14.8	-16.6	-18.0	-19.6	-21.7	-22.9	-23.9	-24.7	-25.0	-24.1	dB
Input Power for 1dB Compression (Reference State)	29.5	29.7	29.9	29.7	29.8	29.7	29.8	30.4	29.7	29.7	dBm
Test Conditions: Pin=0dBm，Temp=+25℃											



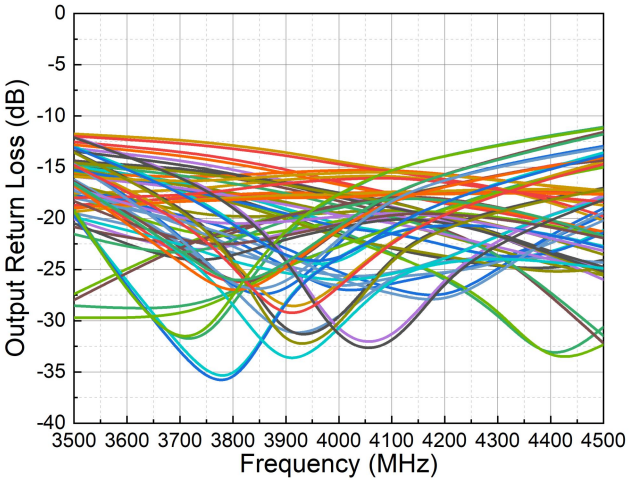
All-State Insertion Loss vs. Freq



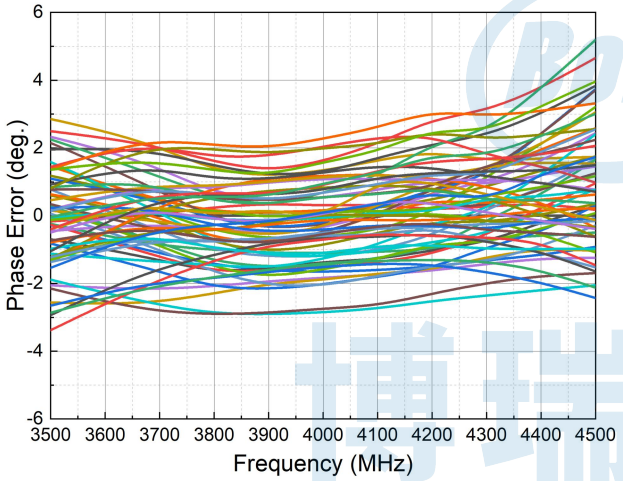
All-State Phase-Shift Amplitude Variation vs. Freq



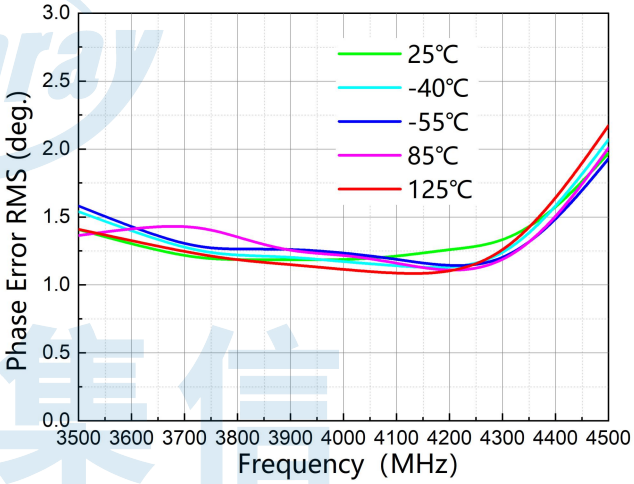
All-State Input Return Loss vs. Freq



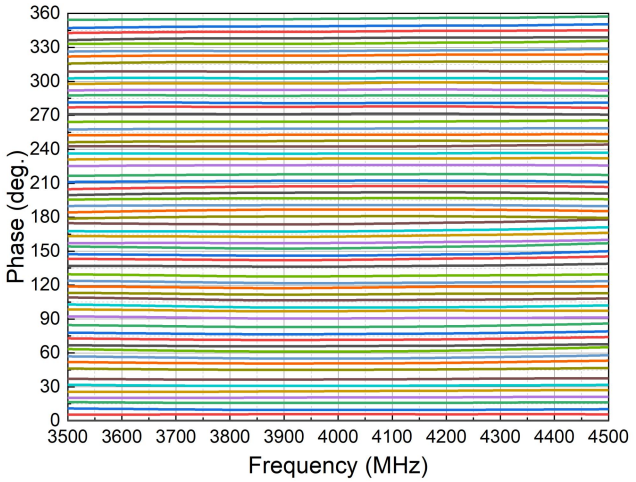
All-State Output Return Loss vs. Power



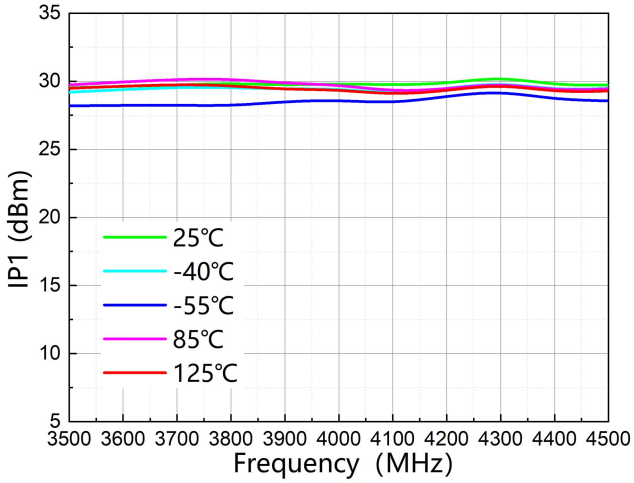
All-State Phase Error vs. Freq



RMS Phase Error vs. Freq

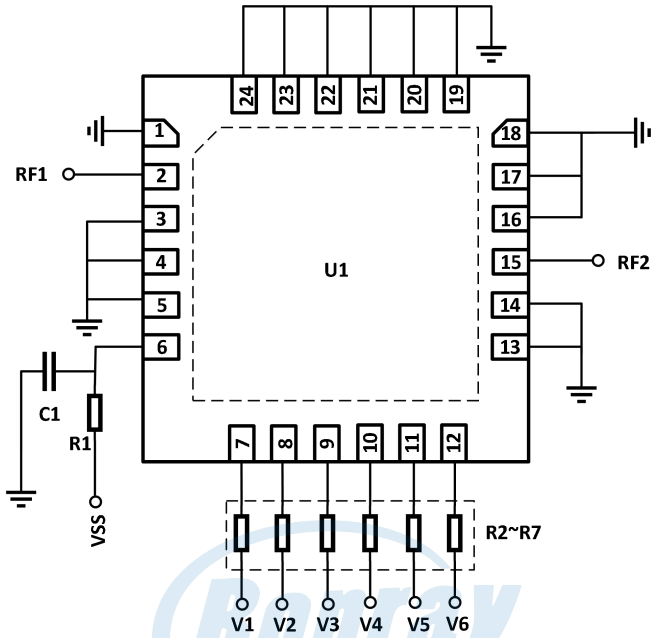


All -State Phase Shift vs. Freq



Reference-State IP1 vs. Freq

Typical Application Schematic



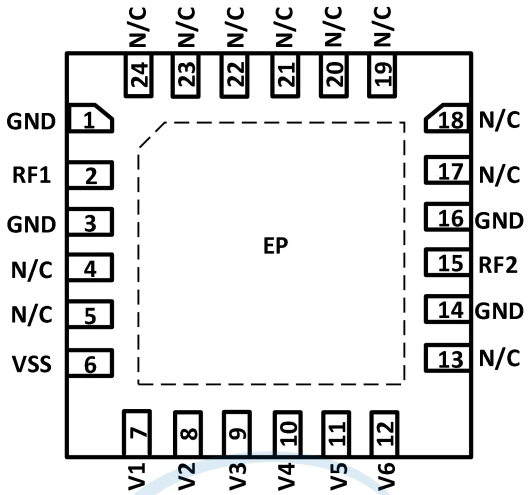
Bill of Material

Designator	Package	Description	Part Number
U1	QFN24	/	BR9597FPJ
R1	0402	0Ω	RC0402FR-070RL
R2~R7	0402	1.3KΩ	RC0402JR-071K3L
C1	0402	1nF	GRM1555C1H102JA01D

Truth Table

State	5.625°	11.25°	22.5°	45°	90°	180°
	V1	V2	V3	V4	V5	V6
Reference State	0	0	0	0	0	0
5.625°	1	0	0	0	0	0
11.25°	0	1	0	0	0	0
22.5°	0	0	1	0	0	0
45°	0	0	0	1	0	0
90°	0	0	0	0	1	0
180°	0	0	0	0	0	1
“0” level range: 0~0.5V；“1” level range: 2.7~5V						

Pin Configuration and Description

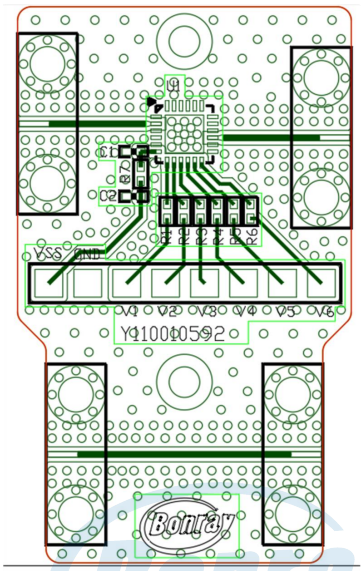


Pin Configuration

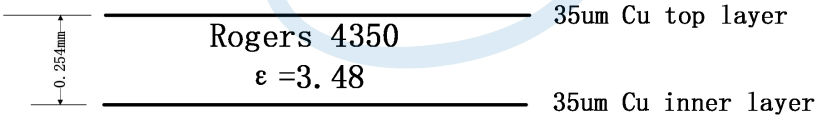
Pin Description

Pin Number	Pin Name	Description
6	VSS	Voltage supply Pin.
2,15	RF1，RF2	RF Pin, DC-coupled and matched to 50 Ω. If the RF potential is not 0 V, an external DC-blocking capacitor is required.
7~12	V1～V6	Control Input Pin. The control logic is detailed in the truth table.
1,3,14,16	GND	Ground Pin. Exposed ground paddle must be connected to RF/DC ground
4、5、13、17~24	NC	No Internal Connection. It is recommended to connect to RF/DC ground without affecting performance.
-	EP	The exposed backside pad must be properly grounded during use.

PCB Evaluation Board



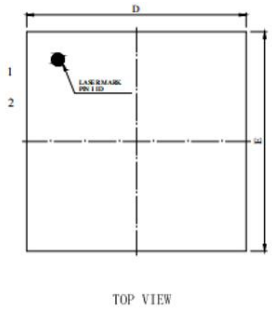
PCB



50Ω line：width=0.406mm, spacing=0.33mm,
PCB thickness 0.4mm

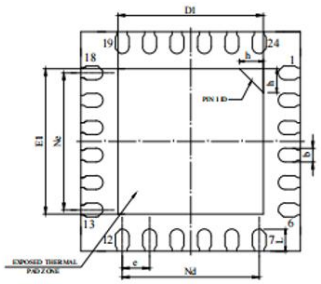
Evaluation Board Information

Package Dimensions (mm)



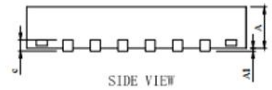
TOP VIEW

SIDE VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
D	3.90	4.00	4.10
D1	2.60	2.70	2.80
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E1	2.60	2.70	2.80
L	0.35	0.40	0.45
h	0.30	0.35	0.40



SIDE VIEW