

Product Features

- Frequency: 1.6GHz ~ 2.3GHz
- Phase Shift Range: 360° , LSB=5.625°
- Insertion Loss: 3.8dB@2GHz
- Input Return Loss: 14.9dB@2GHz
- RMS Phase Error:1.9°
- Supply Voltage: -5V
- Control Voltage: 0/+5V
- Package: QFN32 (5mm*5mm)

Apply

- Communication Base Station
- Radar
- Phased Array

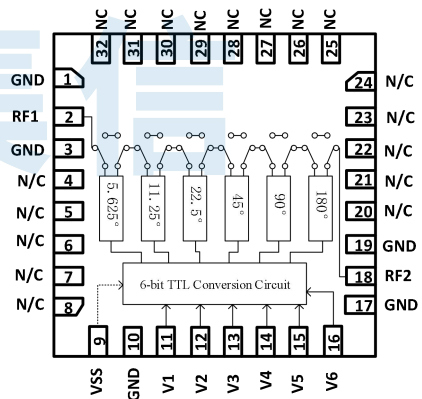
General Description

The BR9595FLJ is a 6-Bit Parallel Digital-Controlled Phase Shifter chip covering a frequency range of 1.6 GHz to 2.3 GHz. It features 0 V / +5 V logic control and requires an external -5 V supply for bias. Providing 360 degrees of phase coverage, with a LSB of 5.625 degrees. It features a typical RMS phase error of 1.4 and a typical insertion loss of 4.6 dB. It is suitable for a wide range of applications including communication base stations, Radar, and Phased Array systems.

Ordering Information

Part Number	Package	Description
BR9595FLJ	QFN32	1.6GHz ~ 2.3GHz 6-Bit Parallel Digital-Controlled Phase Shifter

Functional Block Diagram



Electrical Specifications (Temp=+25°C)

Parameters	Test condition	Min.	Typ.	Max.	Units
Insertion Loss (Reference State)	1600MHz	-	-3.78	-	dB
	2000MHz	-	-3.81	-	
	2300MHz	-	-3.81	-	
Input Return Loss (Reference State)	1600MHz	-	-16.0	-	dB
	2000MHz	-	-14.9	-	
	2300MHz	-	-14.4	-	
Output Return Loss (Reference State)	1600MHz	-	-19.4	-	dB
	2000MHz	-	-18.6	-	
	2300MHz	-	-18.1	-	
Phase Shift Amplitude Modulation	1600MHz	-1.0	-	0.3	dB
	2000MHz	-0.8	-	0.3	
	2300MHz	-0.7	-	0.4	
RMS Phase Error	1600MHz	-	1.7	-	°
	2000MHz	-	1.9	-	
	2300MHz	-	2.5	-	
Input Power for 1dB Compression (Reference State)	1600MHz	-	29.1	-	dBm
	2000MHz	-	30.0	-	
	2300MHz	-	30.1	-	

Absolute Maximum Ratings

Maximum RF Input Power: +30dBm

Maximum Supply Voltage: -5.5V

Recommended Operating Conditions

Control Voltage Threshold: 0~0.5V (“0” level)

2.7V~5V (“1” level)

Control Current: 1.1mA@5V

Storage Temperature: -65°C~+150°C

Operating Temperature: -55°C~+125°C

Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and exposure to absolute-maximum-ratings conditions for extended periods will affect the reliability.

ESD WARNING

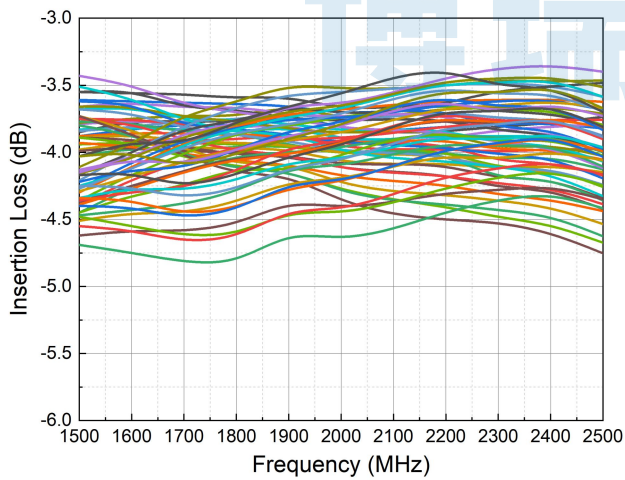
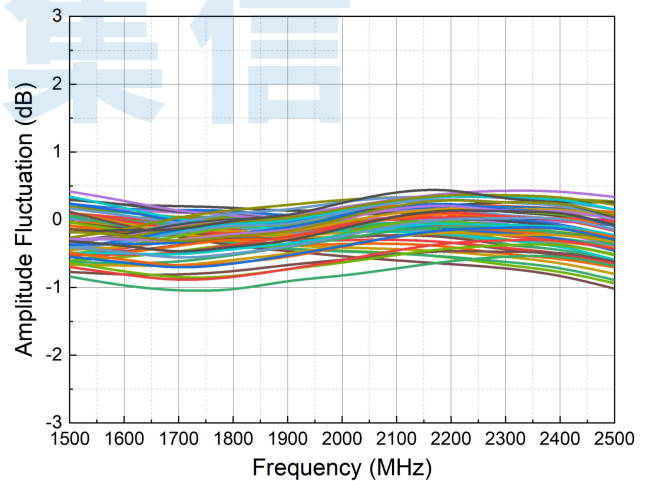
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

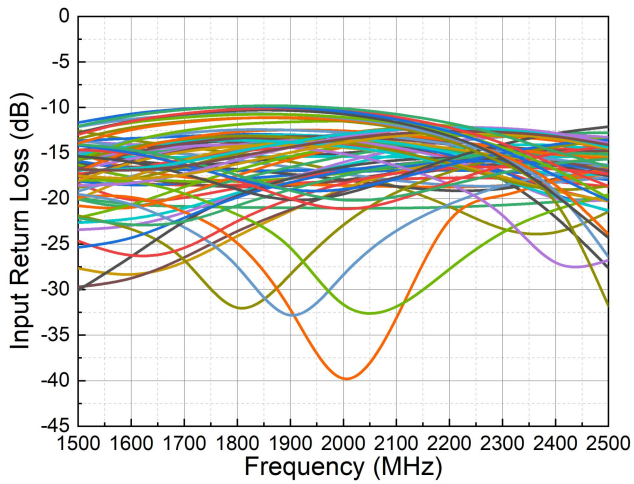
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Typical Performance (Temp=+25°C, EVB Test Results)

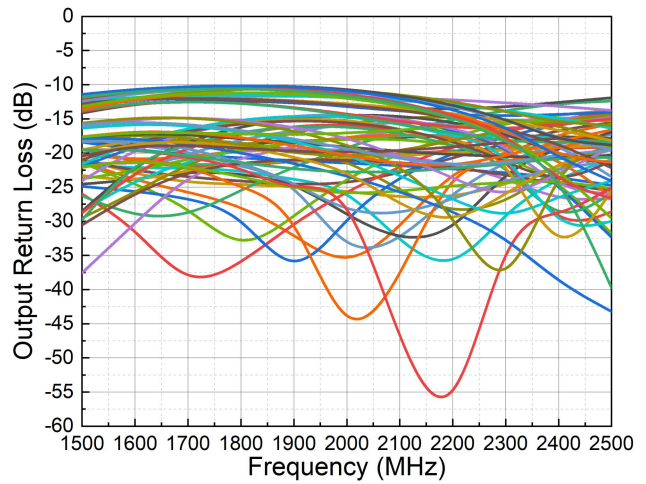
Parameters	Typ.							Units
	1600	1700	1800	1900	2000	2200	2300	
Frequency	1600	1700	1800	1900	2000	2200	2300	MHz
Phase Error (5.625°)	-0.19	-0.05	-0.01	-0.06	-0.02	0.06	0.14	°
Phase Error (11.25°)	-0.46	-0.63	-0.74	-0.78	-0.85	-0.81	-0.55	°
Phase Error (22.5°)	-0.33	-0.51	-0.70	-0.70	-0.85	-0.77	-0.33	°
Phase Error (45°)	-0.72	-1.30	-1.66	-1.60	-1.71	-0.85	0.17	°
Phase Error (90°)	1.57	1.29	1.07	0.90	1.04	1.71	2.44	°
Phase Error (180°)	-1.98	-0.82	-0.51	-0.31	-0.93	-2.49	-3.54	°
Insertion Loss (Reference State)	-3.78	-3.77	-3.76	-3.74	-3.81	-3.84	-3.81	dB
Input Return Loss (Reference State)	-16.0	-15.9	-15.6	-15.2	-14.9	-14.4	-14.4	dB
Output Return Loss (Reference State)	-19.4	-19.7	-19.5	-19.0	-18.6	-18.1	-18.1	dB
Input Power for 1dB Compression (Reference State)	28.9	29.2	29.5	29.6	29.8	29.9	29.8	dBm

Test Conditions: Pin=0dBm, Temp=+25°C

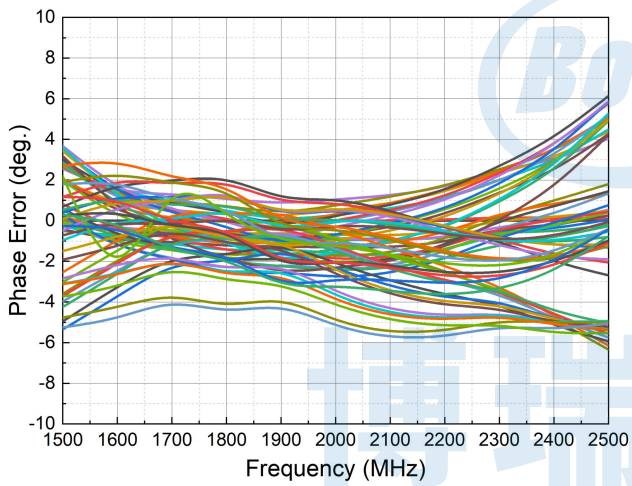

All-State Insertion Loss vs. Freq

All-State Phase-Shift Amplitude Variation vs. Freq



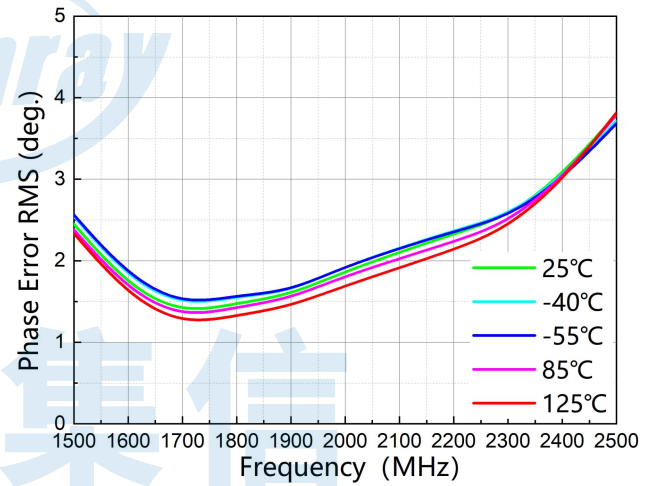
All-State Input Return Loss vs. Freq



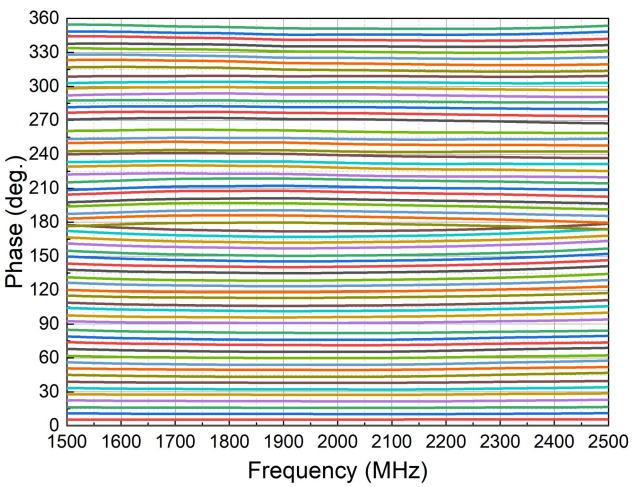
All-State Output Return Loss vs. Power



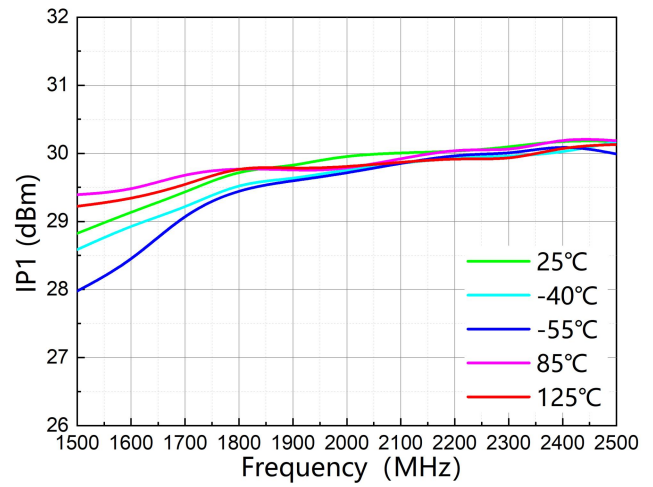
All-State Phase Error vs. Freq



RMS Phase Error vs. Freq

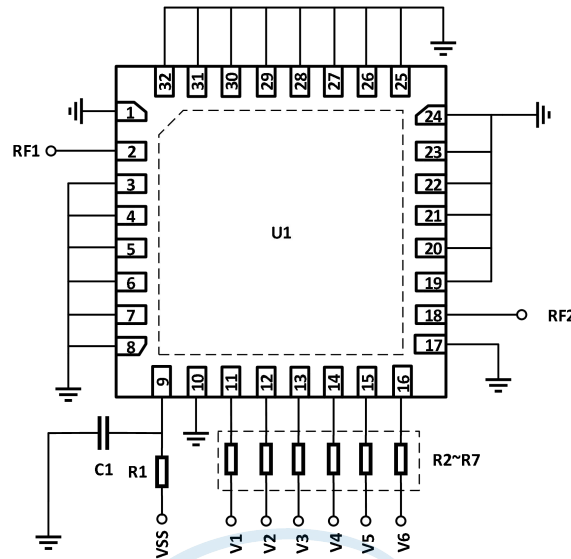


All-State Phase Shift vs. Freq



Reference-State IP1 vs. Freq

Typical Application Schematic



Bill of Material

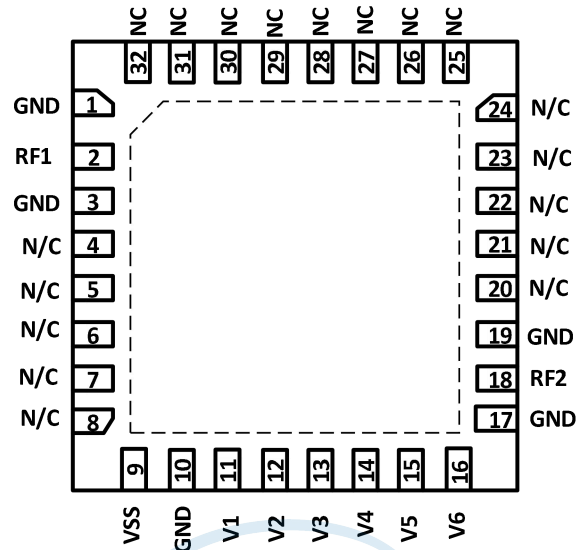
Designator	Package	Description	Part Number
U1	QFN32	/	BR9595FLJ
R1	0402	0Ω	RC0402FR-070RL
R2~R7	0402	1.3KΩ	RC0402JR-071K3L
C1	0402	1nF	GRM1555C1H102JA01D

Note: When R2 through R7 are 1.3 kΩ, the control port draws 1.1 mA at 5 V.

Truth Table

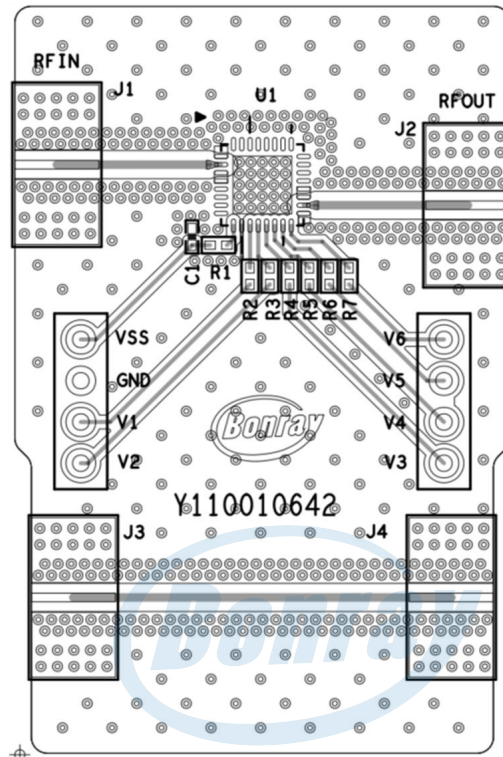
State	5.625°	11.25°	22.5°	45°	90°	180°
	V1	V2	V3	V4	V5	V6
Reference State	0	0	0	0	0	0
5.625°	1	0	0	0	0	0
11.25°	0	1	0	0	0	0
22.5°	0	0	1	0	0	0
45°	0	0	0	1	0	0
90°	0	0	0	0	1	0
180°	0	0	0	0	0	1

“0” level range: 0~0.5V; “1” level range: 2.7~5V

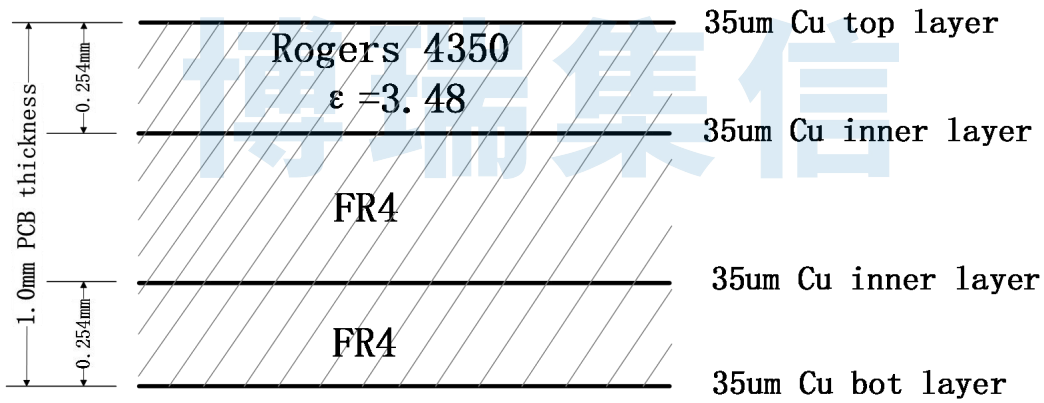
Pin Configuration and Description

Pin Configuration
Pin Description

Pin Number	Pin Name	Description
2, 18	RF1, RF2	RF Pin, DC-coupled and matched to 50 Ω. If the RF potential is not 0 V, an external DC-blocking capacitor is required.
9	VSS	Voltage supply Pin.
11~16	V1~V6	Control Input Pin. The control logic is detailed in the truth table.
1,3,17,19	GND	Ground Pin. Exposed ground paddle must be connected to RF/DC ground
4~8,20~32	NC	No Internal Connection. It is recommended to connect to RF/DC ground without affecting performance.
-	EP	The exposed backside pad must be properly grounded during use.

PCB Evaluation Board



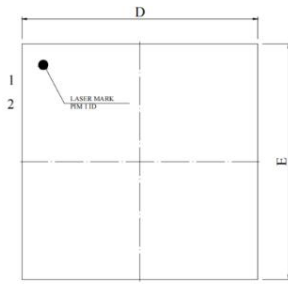
PCB



50 Ω line: width=0.53mm, spacing=0.6mm

Evaluation Board Information

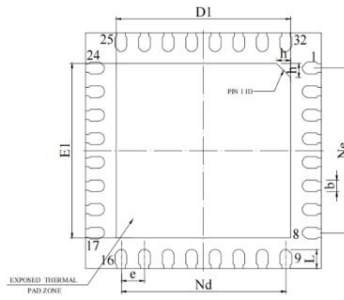
Package Dimensions (mm)



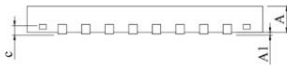
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
D	4.90	5.00	5.10
D1	3.60	3.70	3.80
e	0.50BSC		
Ne	3.50BSC		
Nd	3.50BSC		
E	4.90	5.00	5.10
E1	3.60	3.70	3.80
L	0.35	0.40	0.45
h	0.25	0.30	0.35



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