Product Features

Operating Frequency:3.5GHz～6GHz

Gain:22.0dB@5GHz

Psat: 33.9dBm@5GHz

PAE: 34.1%@5GHz

Operation Voltage: 8V, static current 700mA

Package: QFN20 (5mm x 5mm)

Application

Communication

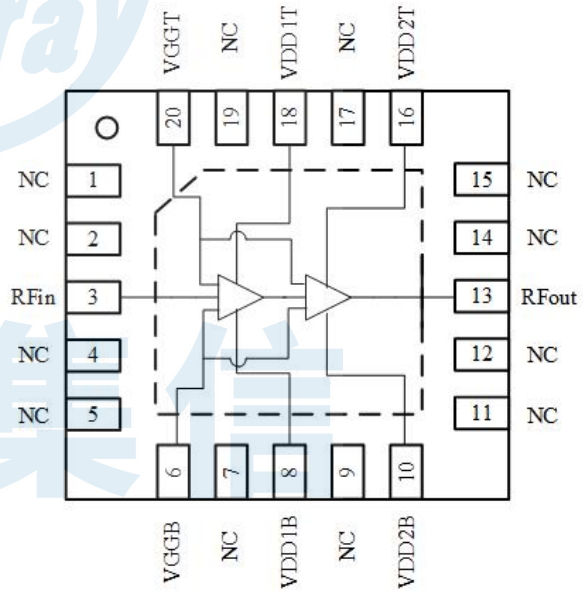
Data Link

Radar

General Description

The BR9217FAJ is a high-linearity driver amplifier operating over 3.5 GHz to 6.0 GHz. Powered by a +8 V drain supply, it features a quiescent current of 700 mA and high output power. The device is ideal for transmitter systems such as point-to-point communications and data links.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BR9217FAJ	QFN20	3.5GHz～6GHz Drive Amplifier

Technical Specifications（EVB test results+8V, 3.5GHz~6GHz）

Parameters	Test conditions	Min	Typ	Max	Units
Small Signal Gain	3.5GHz	—	23.2	—	dB
	5GHz	—	22.0	—	dB
	6GHz	—	21.1	—	dB
Input Return Loss	3.5GHz	—	-10.4	—	dB
	5GHz	—	-23.5	—	dB
	6GHz	—	-11.4	—	dB
Output Return Loss	3.5GHz	—	-13.3	—	dB
	5GHz	—	-26.6	—	dB
	6GHz	—	-23.3	—	dB
Reverse Isolation	3.5GHz	—	-57.4	—	dB
	5GHz	—	-49.1	—	dB
	6GHz	—	-53.9	—	dB
Output Power for 1dB Compression	3.5GHz	—	33.0	—	dBm
	5GHz	—	33.9	—	dBm
	6GHz	—	33.0	—	dBm
Output Third-Order Interception	3.5GHz	—	41.2	—	dBm
	5GHz	—	40.0	—	dBm
	6GHz	—	36.8	—	dBm
Saturated Output Power	3.5GHz	—	35.0	—	dBm
	5GHz	—	33.9	—	dBm
	6GHz	—	33.7	—	dBm
Operating Voltage	—	—	8	9	V
Quiescent Current	—	—	700	—	mA
Test conditions:Vdd=+8V，OIP3 Fspacing=1MHz（Pout=25dBm/tone），TA=+25℃					

Absolute Maximum Ratings

Maximum Supply Voltage: +9V

Maximum RF input Power:+24dBm

Recommended Operating Conditions

Drain Voltage（V_{DD}）：+8V（Typ）

Drain Static Current（I_{DQ}）：700mA（Typ）

Storage Temperature：-65℃～+150℃

Operating Temperature：-55℃～+85℃

Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and. exposure to absolute-maximum-ratings conditions for extended periods will affect the reliability.

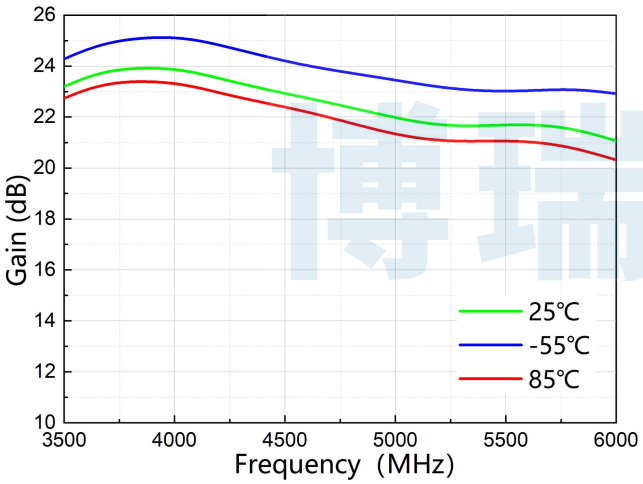
ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

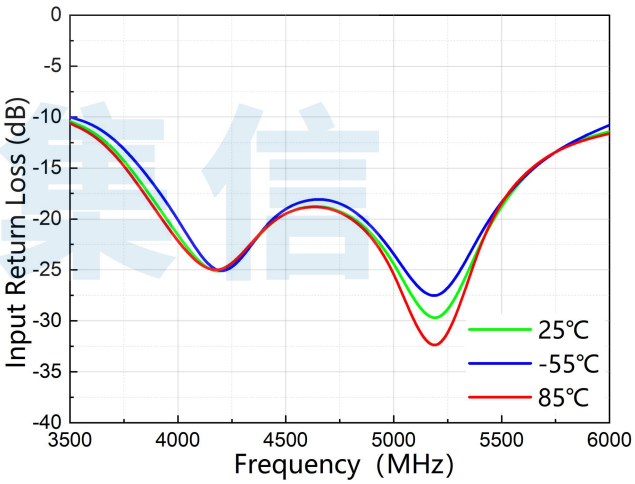
OBSERVE HANDLING PRECAUTIONS

Typical Performance （EVB test results+8V, 3.5GHz~6GHz）

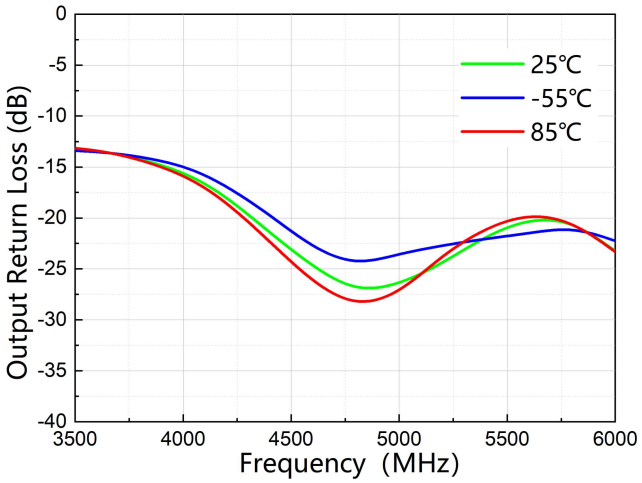
Parameters	Typ.													Unit
Frequency	**3.5**	**3.7**	**4.0**	**4.2**	**4.4**	**4.6**	**4.8**	**5.0**	**5.2**	**5.4**	**5.6**	**5.8**	**6**	**GHz**
Small Signal Gain	23.2	23.9	24	23.5	23.1	22.8	22.4	22	21.7	21.7	21.7	21.6	21.0	dB
Input Return Loss	-10.4	-12.2	-21.8	-27.1	-20.2	-18.4	-19.2	-23.5	-33.2	-21.7	-15.5	-12.6	-11.4	dB
Output Power for 1dB Compression	33.0	32.8	33.6	34.1	34.1	34.5	34.1	33.9	33.7	33.7	33.4	33.9	33.0	dBm
Output Third-Order Interception	41.2	41.1	40.2	39.6	39.6	40	39.9	40	39.8	39.2	38.6	38.2	36.8	dBm
Drain Current@P_{sat}	1043	1043	899	937	919	880	898	890	894	910	945	979	972	mA
Saturated Output Power	35.0	35.0	34.1	34.4	34.2	34.5	34.1	33.9	34.1	34.0	34.0	34.1	33.7	dBm
PAE@P_{sat}	37.1	37	35.1	36.3	35.1	39.8	35.7	34.1	35.5	34.3	32.8	32.4	29.4	%
Power Gain@P_{sat}	17.0	16.0	21.1	21.4	21.2	21.5	20.1	19.9	19.1	19.0	19.0	19.1	17.7	dB
Test Conditions:Temp=+25℃，V_{DD}=8V，I_{DQ}=700mA，OIP3 Fspacing=1MHz（Pout=25dBm/tone）														



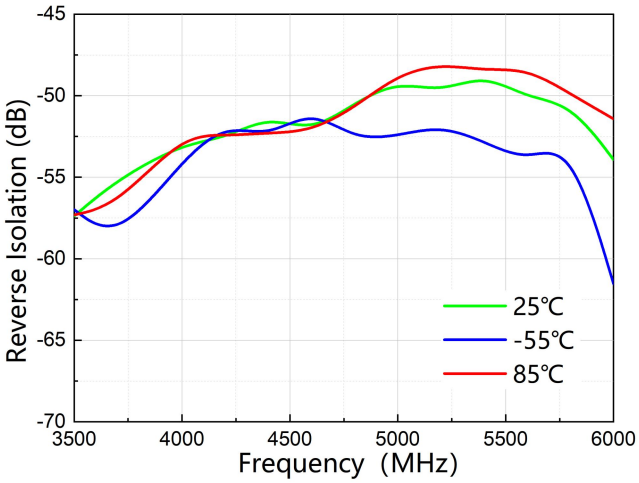
Small Signal Gain vs. Freq



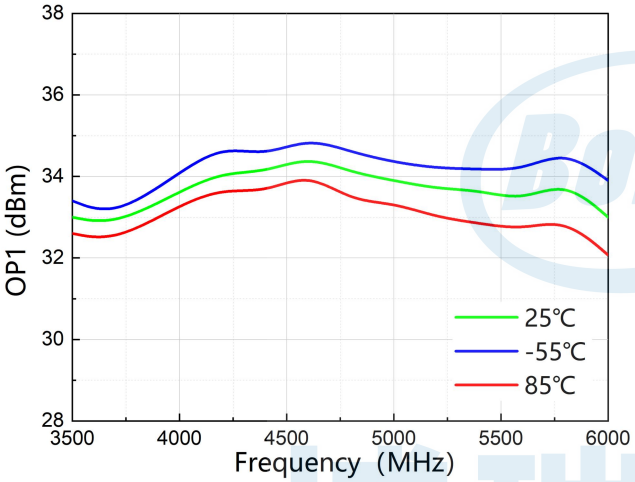
Input Return Loss vs. Freq



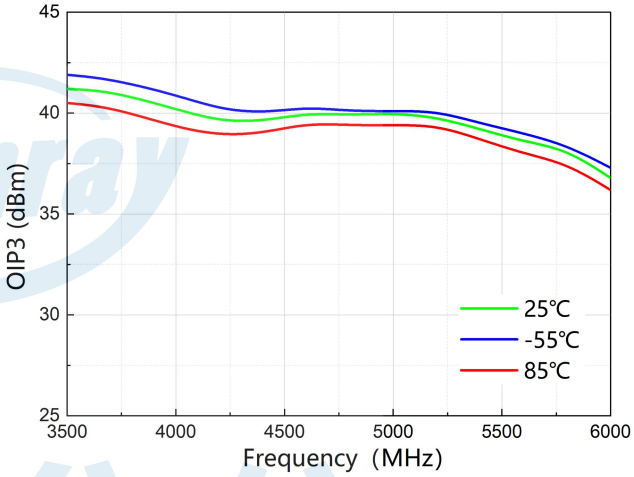
Output Return Loss vs. Freq



Reverse Isolation vs. Freq

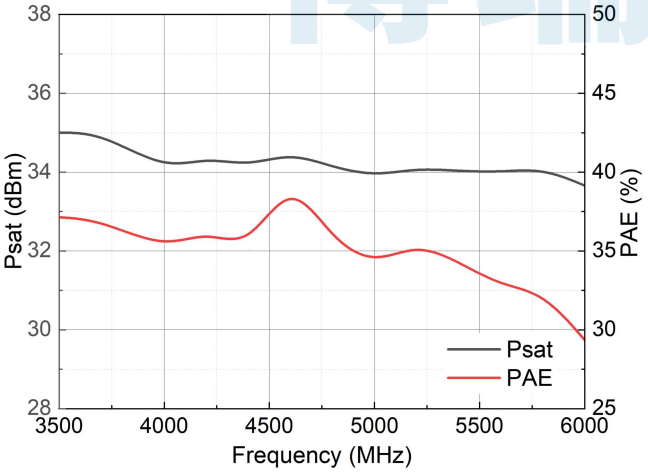


Output Power for 1dB Compression vs. Freq

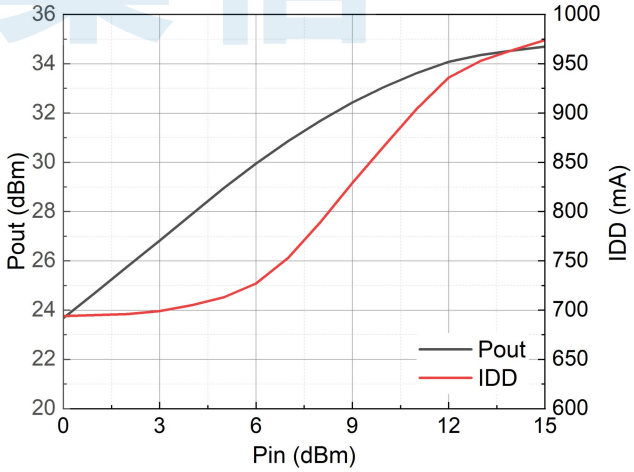


Output Third-Order Interception vs.Freq

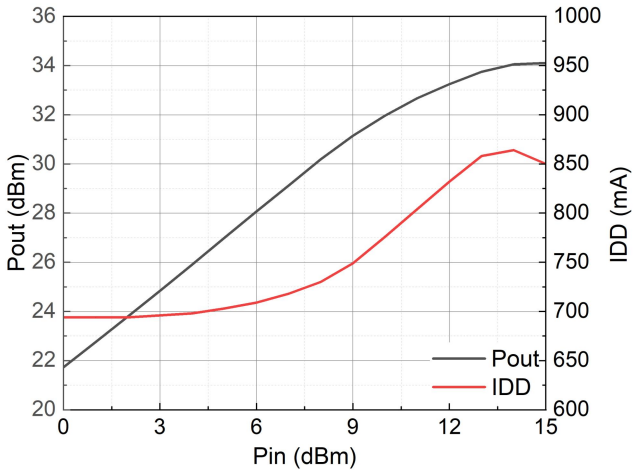
Pout=25dBm/tone，Fspacing=1MHZ



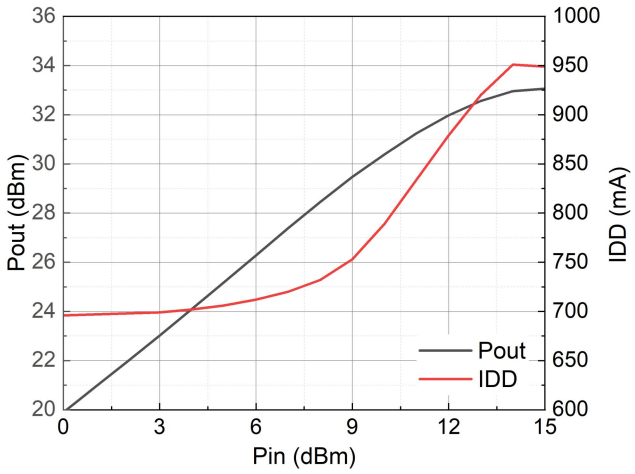
Psat、PAE vs.P_{in}



P_{out}、Idd vs. P_{in} @4GHz

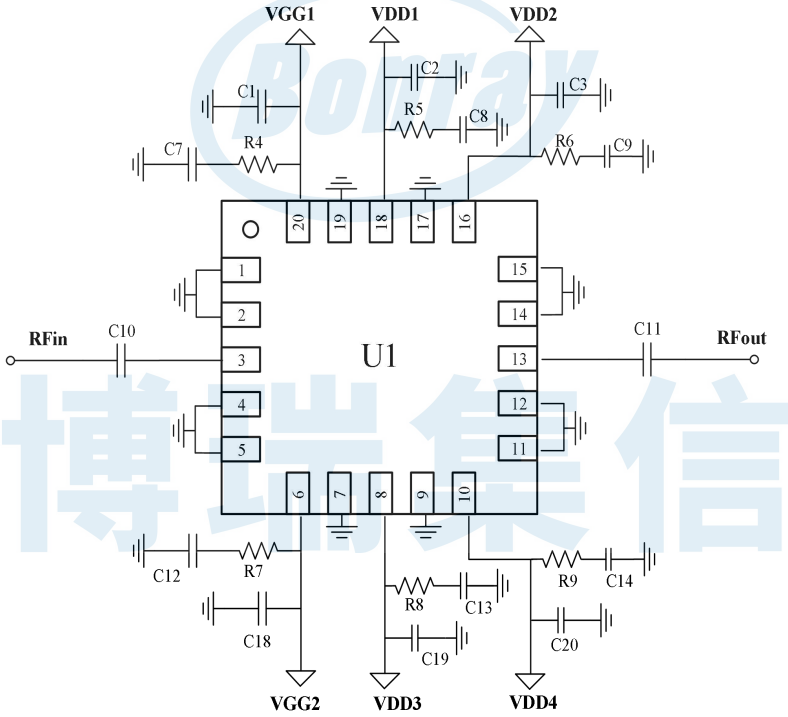


P_{out}、Idd vs. P_{in} @5GHz



P_{out}、Idd vs. P_{in} @6GHz

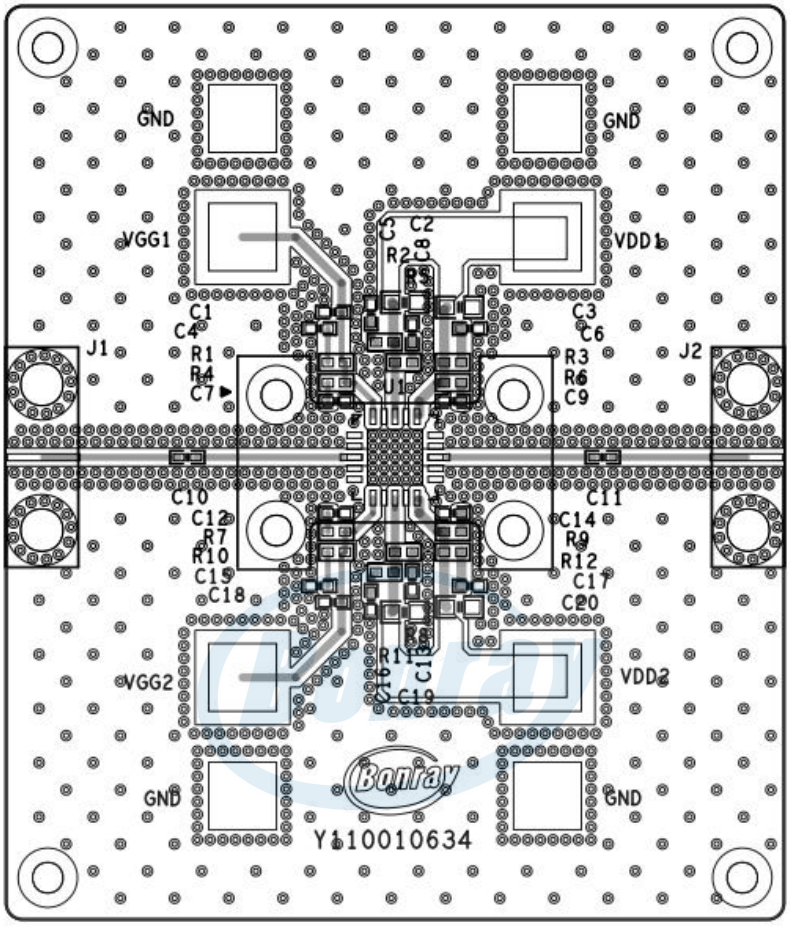
Typical Application Schematic



Bill of Material

Designator	Package	Description	Part Number
C2、C3、C19、C20	C0603	4.7uF	GRM188C71C475KE21D
C1、C18	C0402	2.2uF	GRM155C71A225KE11D
C7、C8、C9、C12、C13、C14	C0402	0.1uF	CL05B104KO5NNNC
R4、R5、R6、R7、R8、R9	R0402	2 Ω	RC0402JR-072RL
C10、C11	C0402	100pF	GRM1555C1H101JA01D

PCB Evaluation Board（10mil Rogers 4350B，double-layer board）



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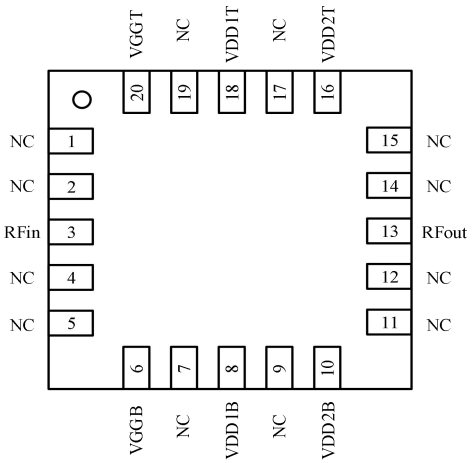
PCB Design Specification

1.The backside pad of the chip is used for RF grounding and heat dissipation. A sufficient number of ground vias shall be provided at the corresponding location (e.g., ground vias with 0.3 mm diameter, quantity ≥ 25), as shown in the figure above.

2.To ensure excellent heat dissipation and grounding performance, it is recommended to connect the bottom layer of the PCB to an external heat dissipation structure using thermal silicone grease.

3.Screws shall be provided around the chip to secure it to the structural components.

Pin Configuration and Description



Pin Number	Pin Name	Description
1、2、4、5、7、9、11、12、14、15、17、19	NC	No connection inside the pin
3	RFin	Rf input, already matched to 50Ω
6、20	VGGB、VGGT	Gate voltage
8、10、16、18	VDD1B、VDD2B、VDD2T、VDD1T	Drain voltage
13	RFout	Rf output, already matched to 50Ω
/	Backside	Backside for the back pad, RF ground and heat dissipation

Power-on Sequence

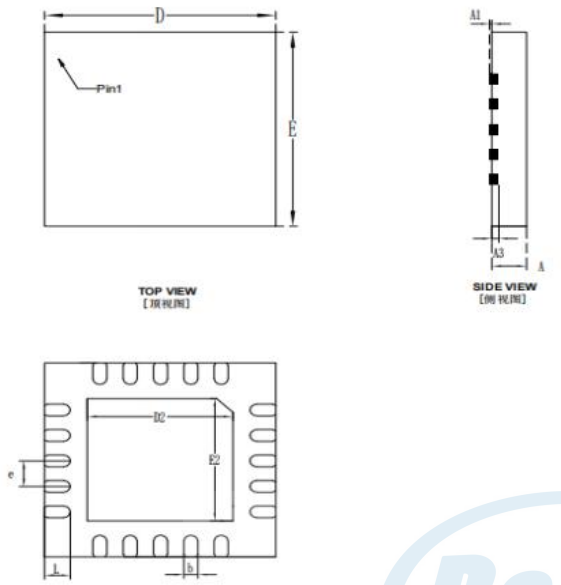
1. Set the gate voltage (V_{GG}) to -3V
2. Set drain voltage (V_{DD}) to +8V with 2.0A current limit
3. Turn on the gate voltage;
4. Turn on the drain voltage
5. Increase the gate voltage (V_{GG}) so that the drain current is 700mA
6. Input RF signal

Power-off Sequence

1. Turn off the RF signal
2. Reduce the gate voltage (V_{GG}) to -3V
3. Turn off the drain Supply Voltage voltage
4. Turn off the gate Supply Voltage voltage

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.65	0.75	0.85
A1	0	0.02	0.05
A3	0.153	0.203	0.253
b	0.25	0.30	0.35
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.60	0.65	0.70
D2	3.10	3.15	3.20
E2	3.10	3.15	3.20
L	0.50	0.55	0.60

Recommended Soldering Temperature Profile