Product Features

Operating Frequency：DC～20GHz

Insertion Loss：1.4dB@12GHz

Isolation:54dB@12GHz

Input Power for 1dB Compression:
25dBm@12GHz

Switching Time：40ns（ON）
10ns（OFF）

VSS=-5V，Supply Current:1mA

Chip Size：2×1×0.075mm

General Description

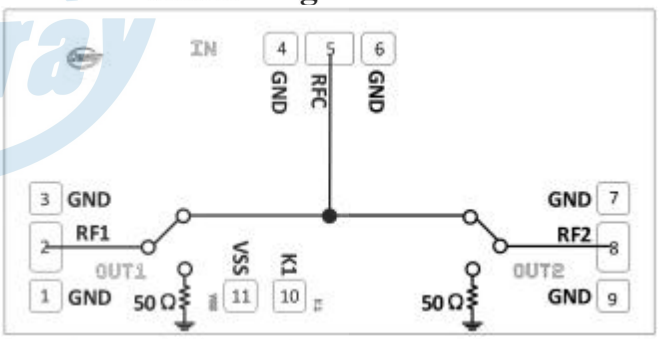
The BR9575LDZ is an absorptive SPDT. It operates within a frequency range from DC to 20GHz, with an integrated TTL control circuit. It employs a -5V power supply and 0/+5V control. This product features a typical insertion loss of 1.4dB and a typical isolation of 54dB.

The device is characterized by small size, low insertion loss, high isolation, fast switching speed, and low DC power consumption. It can be applied in various scenarios such as electronic counter measures and radar systems.

Ordering Information

Part Number	Package	Description
BR9575LDZ	Bare Die	DC～20GHz SPDT Switch

Functional Block Diagram



Electrical Specifications

Parameters	Min	Typ	Max	Unit	Test Conditions
Insertion Loss	-	1	-	dB	1000MHz
	-	1.4	-	dB	12000MHz
	-	2.1	-	dB	20000MHz
Isolation	-	54	-	dB	12000MHz
	-	45	-	dB	20000MHz
Input Power for 1dB Compression	-	26	-	dBm	1000MHz
	-	27	-	dBm	6000MHz
Return Loss（ON）	-	18	-	dB	12000MHz
Return Loss（OFF）	-	19	-	dB	12000MHz
Switching Time Characteristics t_{ON}，（50%CTL-90%RF） t_{OFF}，（50%CTL-10%RF）	-	 40 10	-	ns	 200MHz Pin=0dBm
Test Conditions：VSS=-5V，I=1mA，Vctrl=0/+5V，TA=+25℃					

Absolute Maximum Ratings

Maximum Supply Voltage(VSS)：-5.5V

Maximum RF Input Power：+25dBm

Control Voltage：0V～+5V

Recommended Operating Conditions

Supply Voltage：-5V

Control Voltages：0V～0.5V（Low Level）

4V～5V（High Level）

Supply Current：1mA

Storage Temperature：-65℃~+150℃

Operating Temperature：55℃~+125℃

Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and exposure to absolute-maximum-ratings conditions for extended periods will affect the reliability.

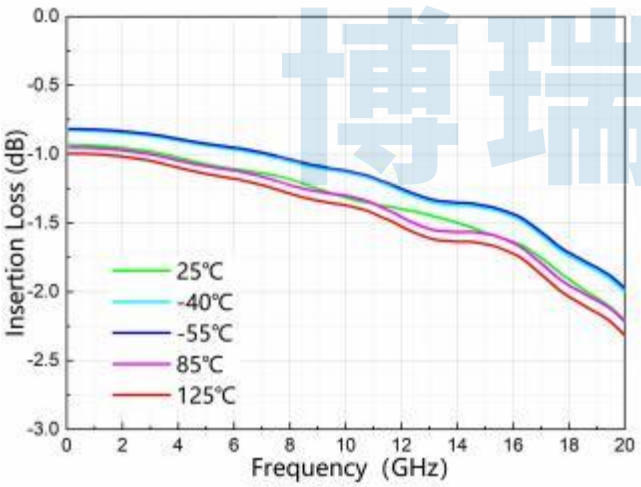
ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

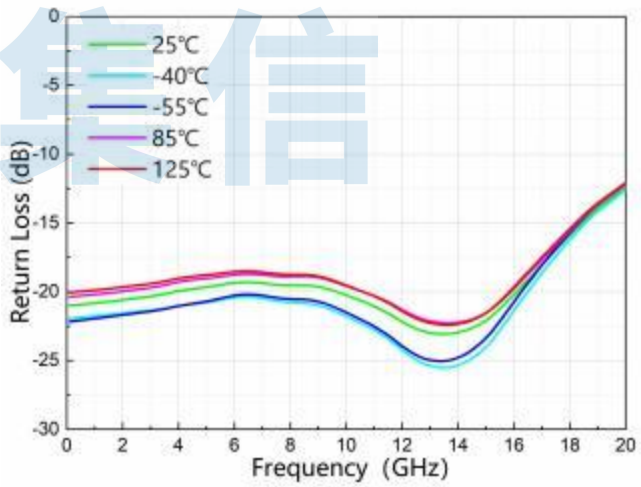
OBSERVE HANDLING PRECAUTIONS

Typical Performance (Probe Test Results)

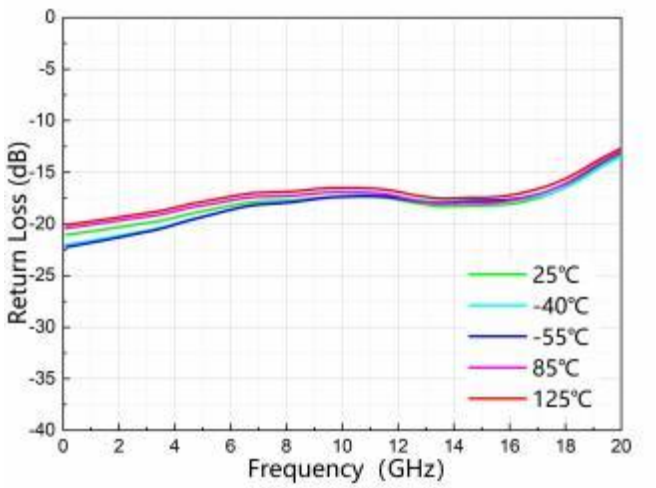
Parameters	Typ											Unit
Frequency	30	500	1000	2000	3000	4000	5000	6000	7000	8000	9000	MHz
Insertion Loss	0.8	0.9	0.9	0.9	1.0	1.0	1.1	1.1	1.1	1.2	1.2	dB
Input RFC Return Loss	21	21.0	20.8	20.6	20.2	20.2	19.6	19.3	19.4	19.6	19.7	dB
Output Return Loss	21.1	21.0	20.7	20.5	19.7	19.6	18.8	18.1	18.0	17.7	17.6	dB
Path Isolation	88.1	73.5	70.0	63.4	60.2	58.5	57.0	55.7	54.7	54.1	53.9	dB
Port Isolation	74.5	72.6	68.6	62.6	59.2	57.4	56.3	55.1	53.6	53.2	52.1	dBm
Frequency	10000	11000	12000	13000	14000	15000	16000	17000	18000	19000	20000	MHz
Insertion Loss	1.3	1.3	1.4	1.4	1.5	1.6	1.7	1.7	1.8	2.1	2.1	dB
RFC Return Loss	19.8	21.5	21.9	22.8	23.8	21.8	20.1	18.4	15.6	14.0	12.4	dB
Output Return Loss	17.3	17.2	17.8	18.1	18.4	18.1	17.7	18.2	16.0	14.7	13.4	dB
Path Isolation	54.1	54.0	54.5	53.7	54.0	58.5	64.2	61.0	53.8	51.5	44.9	dB
Port Isolation	51.5	50.4	50.0	49.0	48.0	46.9	45.7	45.6	45.3	43.5	42.6	dBm
Switching Time	40ns Ton					10ns Toff						ns
Test Conditions：VSS=-5V，I=1mA，Vctrl=0/+5V，TA=+25°C												



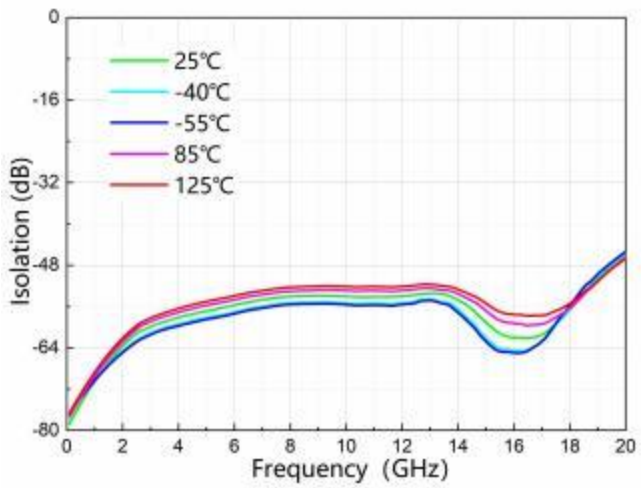
Insertion Loss (RFC to RF1/RF2)



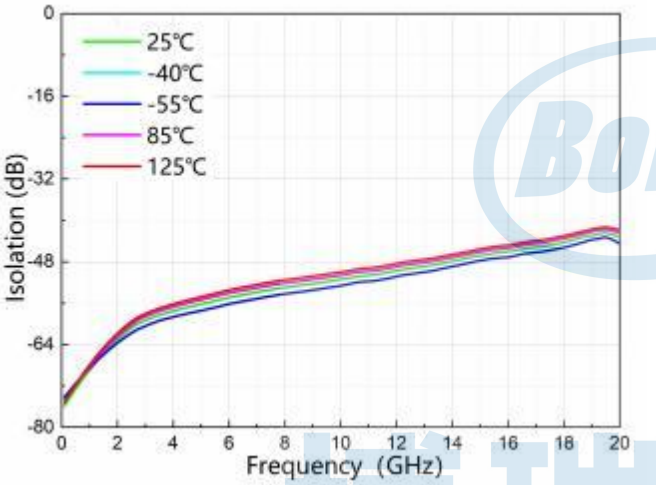
RFC Return Loss



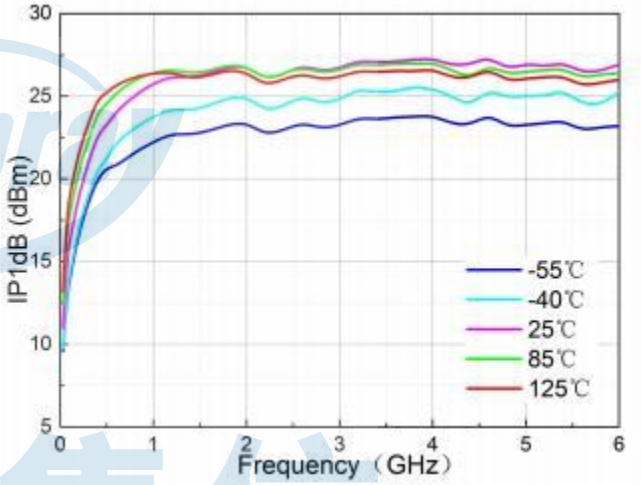
RF1/RF2 Return Loss (ON-State)



Isolation (RFC to RF1/RF2)

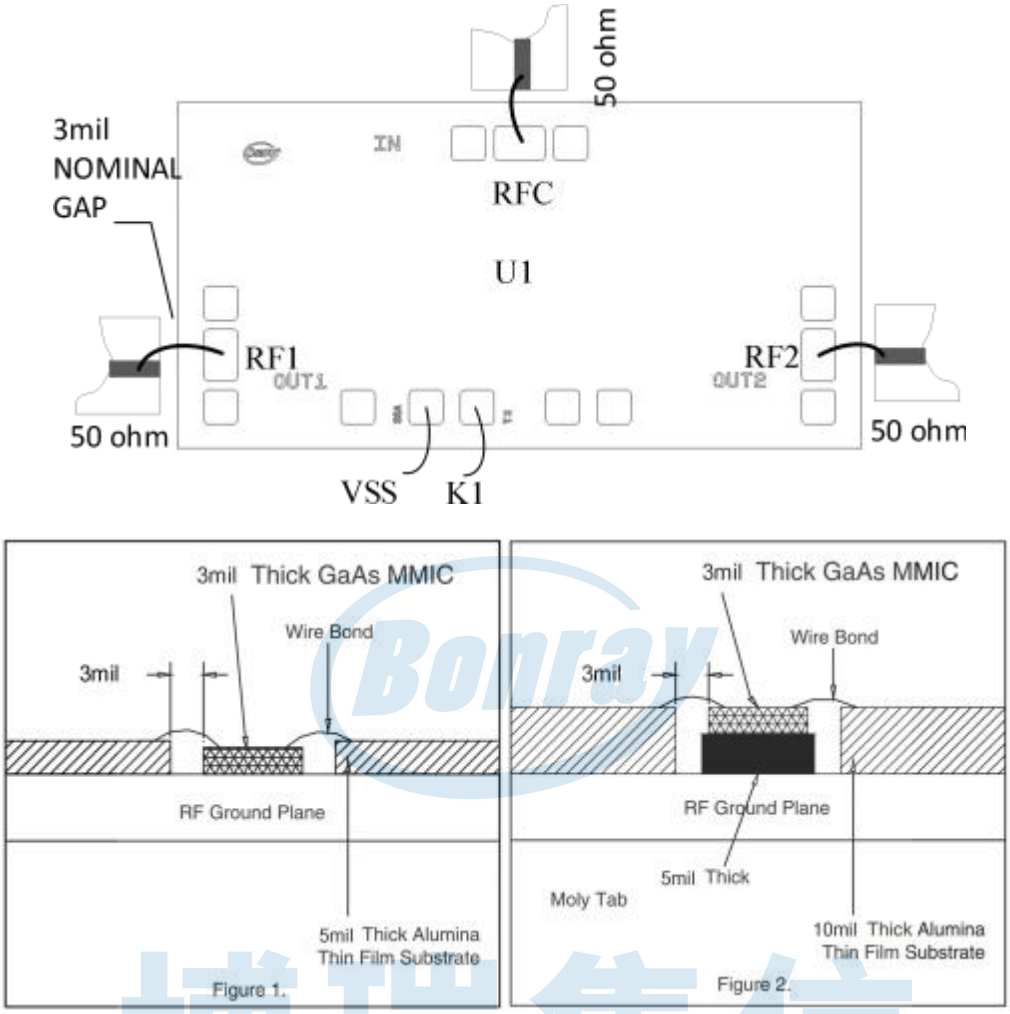


Isolation (RF1 to RF2)



Input Power for 1dB Compression

Assembly Diagram



Assembly Diagram

Notes:

1、It is recommended to connect a 100pF filter capacitor in parallel at the power supply terminal.

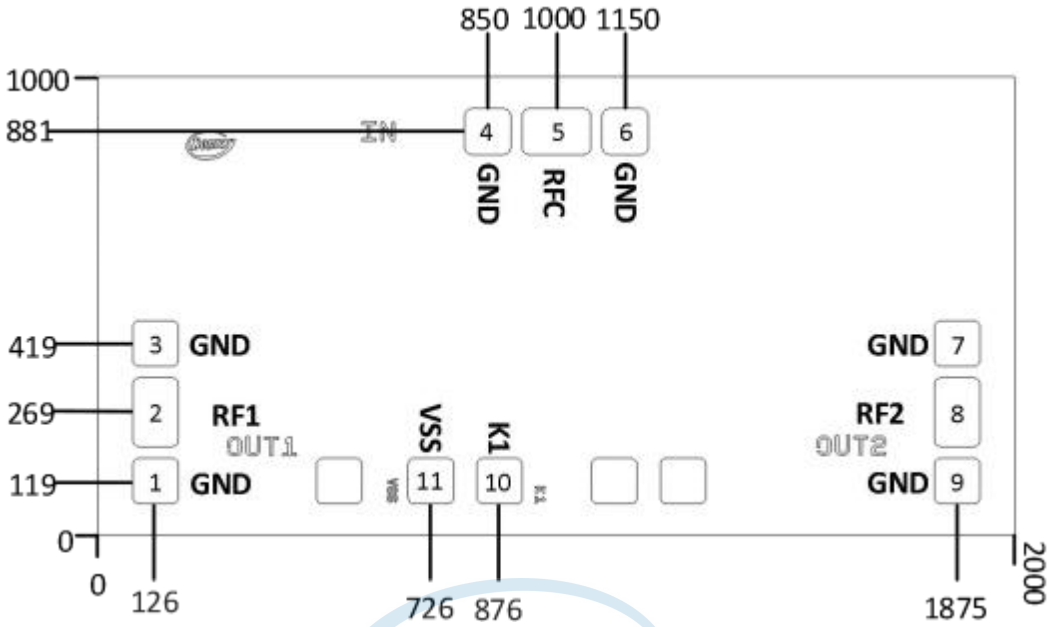
2、For the control input terminal, it is recommended to connect a 100Ω protection resistor in series and a 100pF filter capacitor in parallel.

3、The device itself does not require DC blocking. If there is a DC voltage in the RF channel, an external DC blocking capacitor must be added, and the capacitor should be placed as close as possible to the RF input/output pads.

Important Notice:

1. **Storage:** The chip must be placed in a container with electrostatic protection function, and stored in a nitrogen environment, the temperature is required to 17℃~25℃, the humidity is required to 25%~35%.
2. **Cleaning treatment**: The bare chip must be operated and used in a clean environment. It is forbidden to use liquid cleaning agent to clean the chip.
3. **ESD prevention**: Strictly comply with the requirements of ESD prevention to avoid electrostatic damage.
4. **Routine operation**: Use vacuum pen or precision pointed tweezers to pick up the chip. Avoid touching the chip surface with tools or fingers during operation.
5. **Installation operation**: The chip can be installed by AuSn solder eutectic sintering or conductive adhesive bonding process, the installation surface must be clean and flat, and the gap between the chip and the input and output RF connection line substrate is as small as possible.
6. **Sintering process**: with 80/20AuSn sintering, it is recommended that the peak temperature of sintering does not exceed 300°C, and the maximum temperature duration of sintering does not exceed 5 seconds.
7. **Bonding process**: When using conductive adhesive for bonding, the adhesive effect must meet the requirement of at least 75% adhesive overflow on all four sides, while ensuring the adhesive climb height on all sides does not exceed the chip surface. The curing conditions should follow the specifications provided by the conductive adhesive manufacturer.
8. **Bonding process**: A 25μm gold wire ball bonding process or wedge bonding process is recommended. All bonding wires should be as short as possible, with the first bond on the chip pad and the second bond on the frame/substrate.
9. Die bonding void rate: not more than 10%.
10. Please contact customer service if you have any problem.

Die Outline（Units：um）



Outline Dimensions (Unit: um)

Notes:

1. Backside metal: Gold;
2. Backside is RF and DC ground;
3. The bonding pads are gold-plated,;
4. Bond pads size: RFC/RF1/RF2 pads: 100μm ×150μm,VSS/K1 pads: 100μm × 100μm ;
5. Bonding cannot be performed on through-holes;
6. Die size tolerances: ±50um;
7. Die thickness: 75um.

Functional Description

Pad Numbering	Function Symbols	Functional Description
1,3,4,6,7,9	GND	Grounding Pad; Grounded via through-hole.
5	RFC	RF input pin, internally matched to 50Ω.
2,8	RF1,RF2	RF output pin, internally matched to 50Ω.
11	VSS	Supply Voltage Pin
10	K1	Control input pin; Refer to the control voltage truth table.
Chip Bottom	GND	The bottom of the chip must be well grounded to RF/DC.

Control Voltage Truth Table

Control Input	Signal Flow	
K1	RFC/RF1	RFC/RF2
0	Open	Close
1	Close	Open

Note: 1."0" level range: 0~0.5V; "1" level range: 4~5V.
2.Power-up sequence: First power up VSS, then apply the control signal, followed by the RF signal; the power-down sequence is the reverse of the power-up sequence.