Product Features

Operating Frequency: 2GHz ~ 20GHz

Gain: 16.1dB@10GHz

Noise Figure: 1.7dB@10GHz

Output Third-Order Interception: 28.1dBm@10GHz

Output Power for 1dB Compression: 18.0dBm@10GHz

Supply Current: 70mA @ Vdd=+5V

Die Size: 3.1 x 1.3 x 0.1(mm)

Application

Radar and Electronic Countermeasures

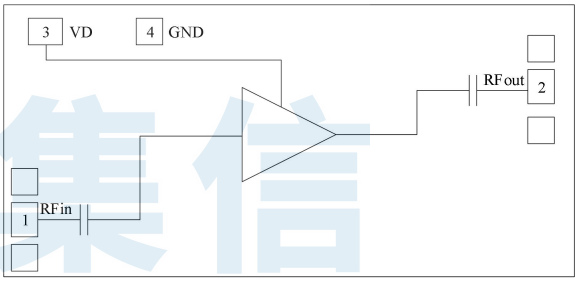
Military and Aerospace

Test Instrumentation

General Description

The BR9614LD is a MMIC gain block amplifier die designed using GaAs process which operates between 2GHz and 20GHz. At 10GHz, the amplifier typically provides a gain of 16.1dB, an output P1dB of 18.0dBm, and a noise figure of 1.7dB under the condition of +5V power supply. It has been internally matched to 50 ohms and AC coupled, thereby eliminating the need for external DC blocks and RF port matching. The BR9614LD amplifier is ideal for integration into Multi-Chip-Modules (MCMs) due to its small size.

Functional Block Diagram



Electrical Specifications

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Gain	2GHz	-	17.6	-	dB
	10GHz	-	16.1	-	dB
	20GHz	-	15.0	-	dB
Output Power for 1dB Compression	2GHz	-	18.8	-	dBm
	10GHz	-	18.0	-	dBm
	20GHz	-	15.5	-	dBm
Output Third-Order Interception	2GHz	-	28.5	-	dBm
	10GHz	-	28.1	-	dBm
	20GHz	-	25.2	-	dBm
Noise Figure	2GHz	-	3.0	-	dB
	10GHz	-	1.7	-	dB
	20GHz	-	4.1	-	dB
Input Return Loss	2GHz	-	-17.5	-	dB
	10GHz	-	-17.8	-	dB
Output Return Loss	2GHz	-	-14.8	-	dB
	10GHz	-	-15.9	-	dB
Supply Voltage	-	-	5	-	V
Supply Current	-	-	70	-	mA
Test Conditions: VDD=+5V, I=70mA, OIP3 spacing=1MHz, Pout=0dBm/tone, TA=+25℃					

Absolute Maximum Ratings

Maximum Operating Voltage: +5.5V

Maximum RF input Power: +15dBm

Recommended Operating Conditions

Supply Voltage: +5V

Supply Current: 70mA

Operating Temperature: -55℃ ~ +125℃

Storage Temperature: -65℃ ~ +150℃

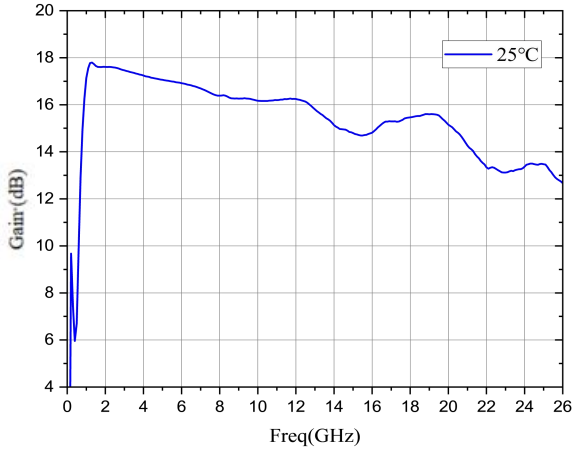
Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and. exposure to absolute-maximum-ratings conditions for extended periods will affect the reliability.

ESD WARNING

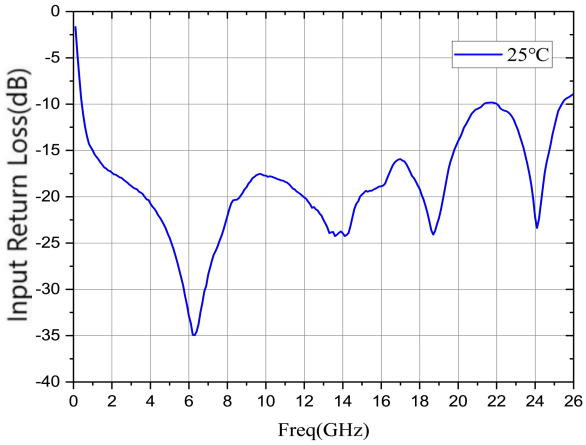
ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

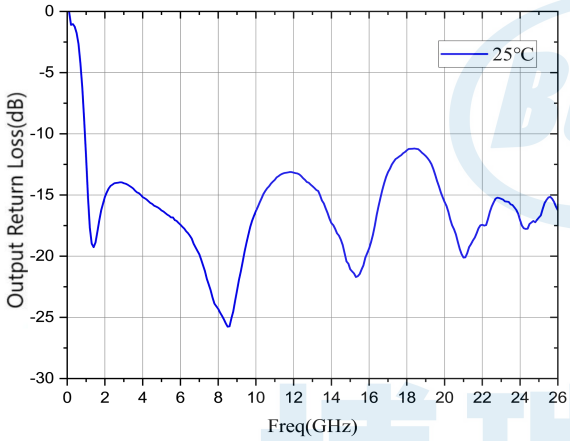
Typical Performance (VDD=+5V, TA=+25℃)



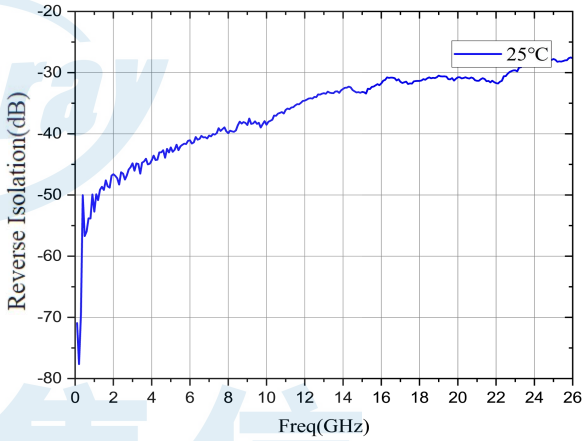
Gain



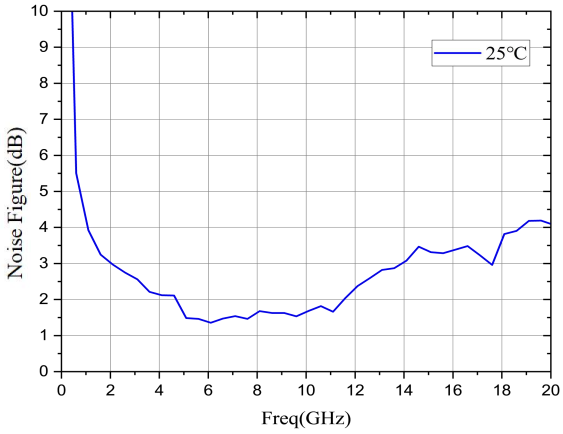
Input Return Loss



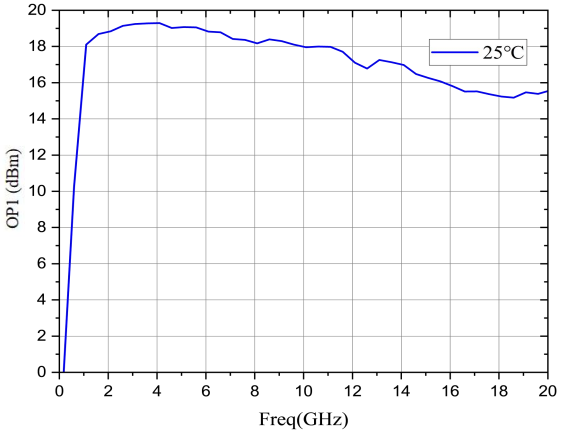
Output Return Loss



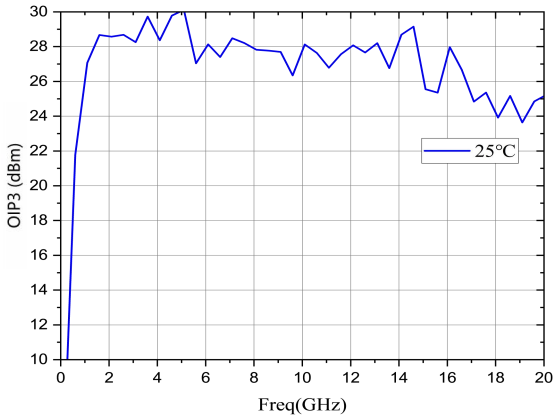
Reverse Isolation



Noise Figure

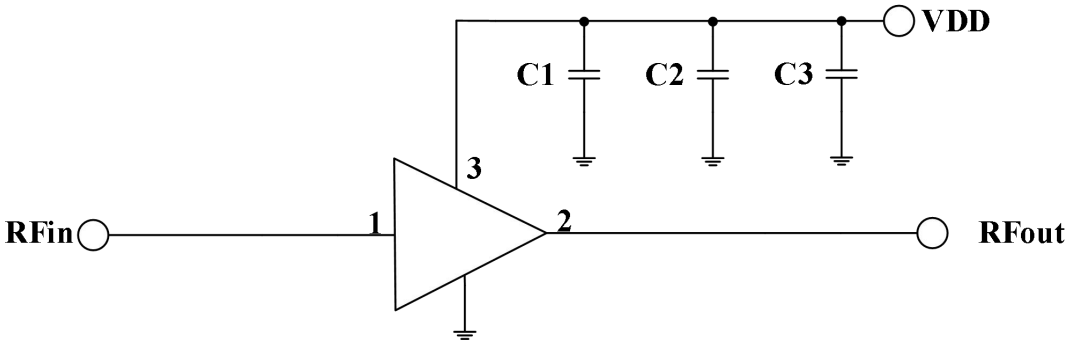


Output Power for 1dB Compression



Output Third-Order Interception

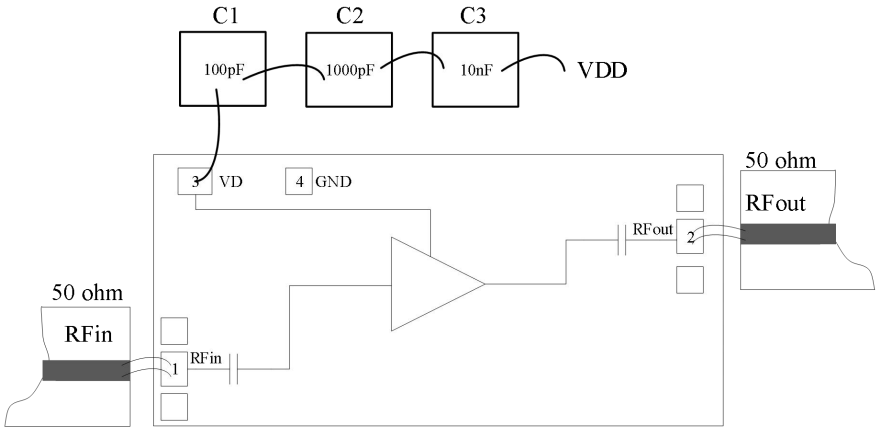
Typical Application Schematic



Bill of Material

Designator	Package	Description	Part Number
C1	Chip Capacitor	100pF	SG201N101MSTW
C2	Chip Capacitor	1000pF	CT91202X102M100TW
C3	Chip Capacitor	10nF	CT91-20-2X-103-M-50-C-W

Assembly Diagram



Handling Precautions：

1. **Storage:** All bare die are placed in ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

2. **Cleanliness**: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

3. **Electrostatic protection:** Follow ESD precautions to protect against ESD strikes

4. **General Handling**: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip should not be touched with vacuum collet, tweezers, or fingers.

5. **Mouning:** The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

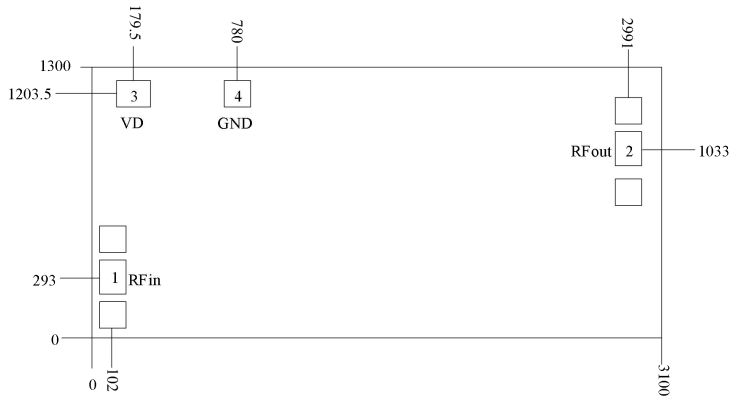
6. **Eutectic Die Attach**: A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment

7. **Conductive epoxy Die Attach:** Apply conductive epoxy to the mounting surface so that the overflow of conductive epoxy on all four sides should not be less than 75%, and the height of conductive epoxy climbing on all four sides should not exceed the surface of the chip. Cure conductive epoxy per the manufacturer's schedule.

8. **Die bonding process unless otherwise noted**: Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate.

9. If you have any questions, please contact customer service.

Mechanical Information（Units：um）



Notes:

1. Backside and bond pad metal: Gold
2. Backside is RF and DC ground
3. Pad size: RFin 125um×100um; RFout 125um×100um; VDD 125um×100um;
4. Cannot be bonded on the hole;

Pad	Description
RFin	RF Input, matched to 50 Ohms.
RFout	RF Output, matched to 50 Ohms.
VDD	Power Supply. See assembly for required external components.
GND	Connected to DC/RF ground.