Product Features

Output Frequency Range: 47MHz～6000MHz

Fractional-N Frequency Synthesizer

Programmable 1/2/4/8/16/32/64 frequency division output

Supply Voltage: 3.3V、1.2V

Dual-Modulus Prescaler: 4/5、8/9

SPI Output

Package: QFN32 (5mm*mm)

Applications

Wireless Infrastructure（W-CDMA、TD-SCDMA、WIMAX、GSM、PCS、DCS、DECT）

Test Equipment

WLAN

CATV Equipment

Clock Generation

FM Modulation

Operating Conditions

Digital Supply Voltage: 3.3V/1.2V

Analog Supply Voltage: 3.3V/1.2V

Operating Temperature: -55℃~+125℃

Storage Temperature: -65℃~+150℃

Product Overview

With an external loop filter and reference clock, the BR9069FLJ implements fractional-N or integer-N PLL frequency synthesis. Typical supply current is 55 mA at 3.3 V and 65 mA at 1.2 V, making it ideal for low-power applications.

The BR9069FLJ integrates a VCO with a fundamental tuning range of 3 GHz to 6 GHz. On-chip divide ratios of 1, 2, 4, 8, 16, 32, or 64 extend the RF output down to 47 MHz. All registers are programmed via a standard SPI interface, and the device operates from 3.3 V and 1.2 V supplies.

Functional Block Diagram

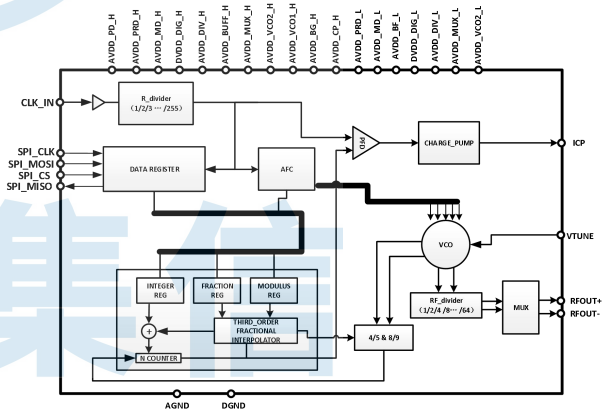


Figure 1. Functional Block Diagram

Ordering Information

Table 1. Ordering Information

Device Part Number	Package Type	Description
BR9069FLJ	QFN32	47 MHz – 6 GHz Fractional-N PLL with Integrated VCO

Specifications(Unless otherwise specified, AVDD_PD_H=AVDD_PRD_H=AVDD_MD_H=DVDD_DIG_H=AVDD_DIV_H=AVDD_BUFF_H=AVDD_MUX_H=AVDD_VCO2_H=AVDD_VCO1_H=AVDD_BG_H=AVDD_CP_H=3.3V±5%, AVDD_PRD_L=AVDD_MD_L=AVDD_BF_L=DVDD_DIG_L=AVDD_DIV_L=AVDD_MUX_L=AVDD_VCO2_L=1.2V±5%. Operating Temperature: T_A=-55℃~+125℃.)

Table 2. Electrical Characteristics

Parameter		Test Conditions	Minimum value	Typical value	Maximum value	Unit
Input Reference Characteristics	Input Frequency		-	-	200	MHz
	Input Sensitivity		0.2	-	1.2	Vp-p
PFD	PFD Frequency		5	-	50	MHz
CP	Current	0.5V≤CPOUT≤2.8V	-	0.4	-	mA
	charge-discharge current mismatch		-	1	-	%
	I_{CP} vs. VTUNE		-	1.5	-	%
	I_{CP} vs. Temperature		-	2	-	%
Logic Inputs	Input High VoltageV		-	3.3	-	V
	Input Low VoltageV		-	0	-	V
Logic Outputs	Output High VoltageVOH		-	3.3	-	V
	Output Low VoltageVOL		-	0	-	V
Supply	AVDD_PD_H=AVDD_PRD_H=AVDD_MD_H=DVDD_DIG_H=AVDD_DIV_H=AVDD_BUFF_H=AVDD_MUX_H=AVDD_VCO2_H=AVDD_VCO1_H=AVDD_BG_H=AVDD_CP_H	-	3.15	3.3	3.45	V
	AVDD_PRD_L=AVDD_MD_L=AVDD_BF_L=DVDD_DIG_L=AVDD_DIV_L=AVDD_MUX_L=AVDD_VCO2_L		1.15	1.2	1.25	V
	Supply Current	REFIN=20MHz、prescaling ratio=1、Ndivision ratio=150、VCO output division ratio=1	-	55@3.3V 65@1.2V	-	mA

RF Output Characteristics	VCO Output Frequency	-	3000	-	6000	MHz
	VCO Sensitivity KVCO	-	-	60	-	MHz/V
	Minimum RF Output Power	Temperature：25℃ RFOUT+/ RFOUT-	-	-3.7	-	dBm
	Maximum RF Output Power		-	4.2	-	dBm
	Minimum VCO Tuning Voltage	-	-	1.45	-	V
	Maximum VCO Tuning Voltage	-	-	1.85	-	V
	PLL Phase-Noise Performance @3GHz PFD Frequency: 20MHz Loop Bandwidth: 80KHz	1 kHz Offset	-	-88	-	dBc/Hz
		10 kHz Offset	-	-91	-	dBc/Hz
		100 kHz Offset	-	-93	-	dBc/Hz
		1 MHz Offset	-	-128	-	dBc/Hz
	PLL Phase-Noise Performance @6GHz PFD Frequency: 20MHz Loop Bandwidth: 80KHz	1kHz Offset	-	-82	-	dBc/Hz
		10 kHz Offset	-	-80	-	dBc/Hz
		100 kHz Offset	-	-82	-	dBc/Hz
		1 MHz Offset	-	-118	-	dBc/Hz

ESD Warning

	ESD (electrostatic discharge) sensitive devices. Charged devices and circuit boards can discharge without notice; high-energy ESD may damage the device. Always use appropriate ESD precautions to prevent performance degradation or loss of functionality.

Timing Characteristics (Unless otherwise specified, AVDD_PD_H=AVDD_PRD_H=AVDD_MD_H=DVDD_DIG_H=AVDD_DIV_H=AVDD_BUFF_H=AVDD_MUX_H=AVDD_VCO2_H=AVDD_VCO1_H=AVDD_BG_H=AVDD_CP_H=3.3V±5%, AVDD_PRD_L=AVDD_MD_L=AVDD_BF_L=DVDD_DIG_L=AVDD_DIV_L=AVDD_MUX_L=AVDD_VCO2_L=1.2V±5%. Operating temperatureT_A=-55℃~+125℃. High-level voltage: 3.3 V, Low-level voltage:0 V, Clock Frequency:fmax=25 MHz, Period:T=40 ns.)

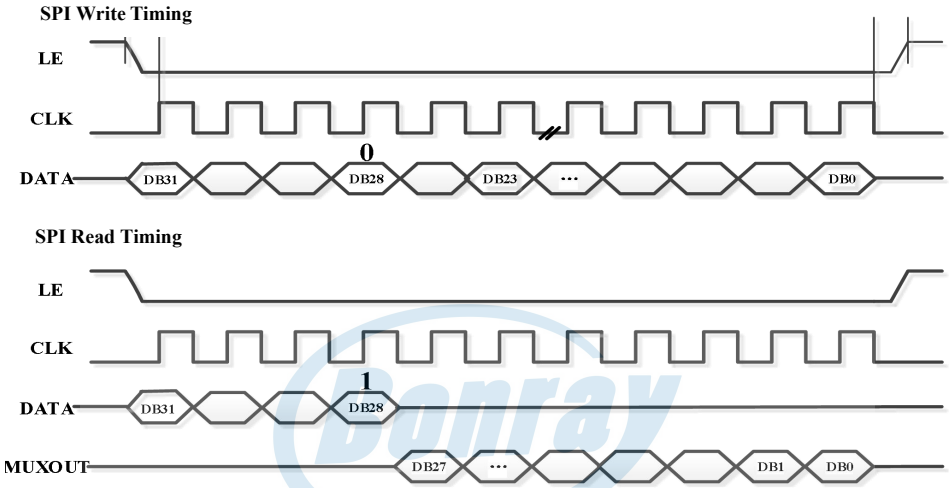


Figure 2. Timing Diagram of SPI Read/Write Operation Modes

Note: 1. Register REG0 must be configured last to refresh all register data.

2. First send the address bits, then the read/write bit, and finally the data bits. The higher bits of the address are sent first, and the higher bits of the data are sent first.

3. The host (master) sends data on the falling clock edge, while the slave receives data on the rising clock edge.

4. The maximum supported SPI clock rate is 25MHz.

5. A minimum interval of 10 clock edges is recommended between register configurations.

6. Ensure the reference signal input is normal before configuration.

Typical Operating Characteristics

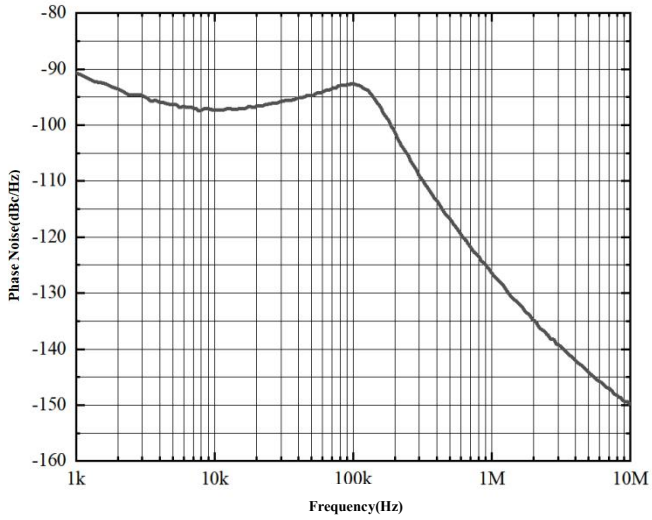


Figure 3. Phase Noise Performance with 100kHz Loop Bandwidth @3GHz

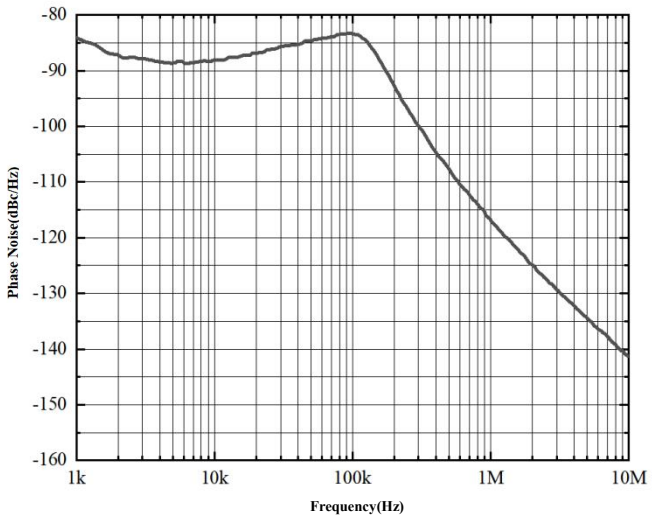


Figure 4. Phase Noise Performance with 100kHz Loop Bandwidth @6GHz

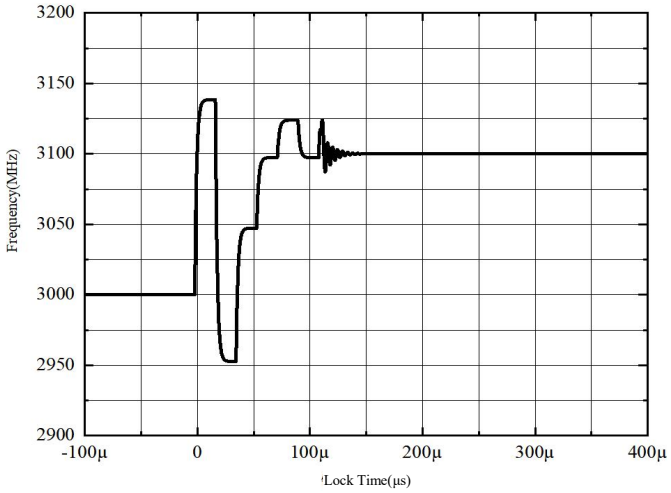


Figure 5. Lock time for 50MHz reference frequency stepping up to 100MHz

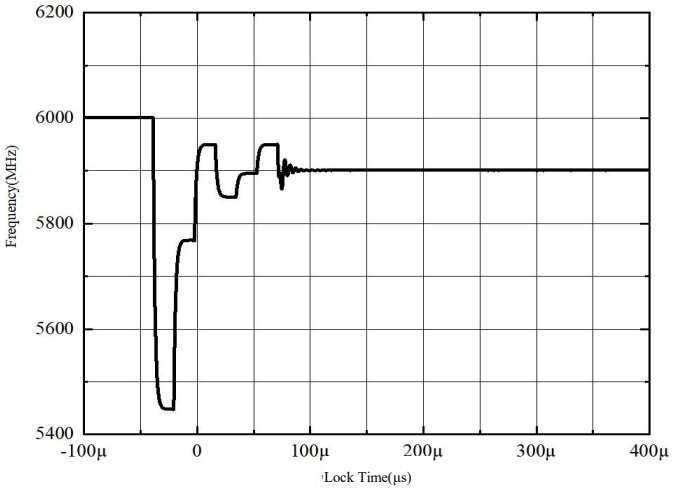


Figure 6. Lock time for 50MHz reference stepping down to 100MHz

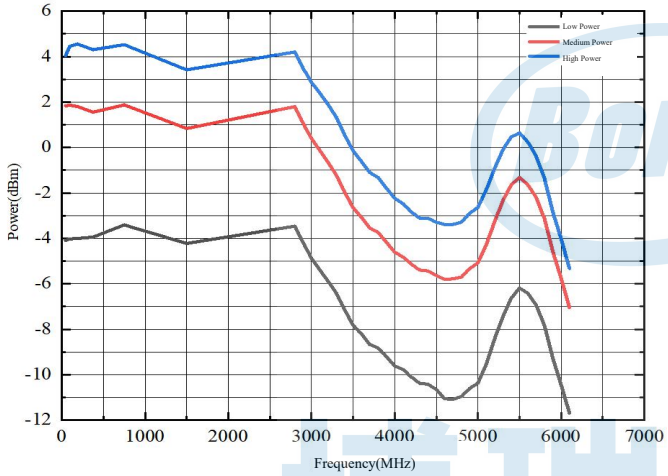


Figure 7. RFOUT+/- RF output power in Three Modes

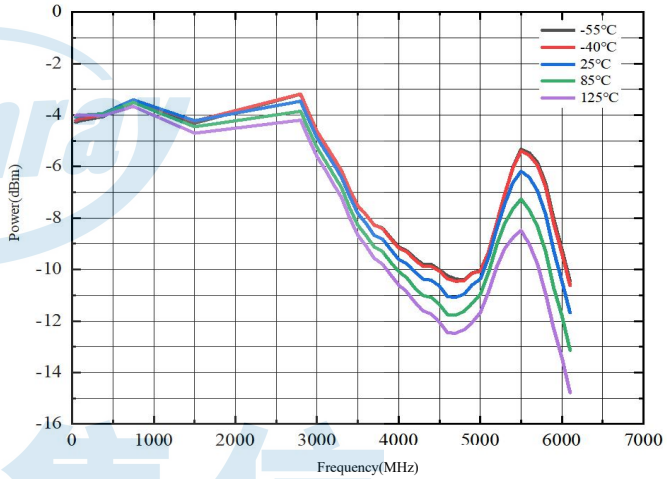


Figure 8. RFOUT+/- RF output low-power mode

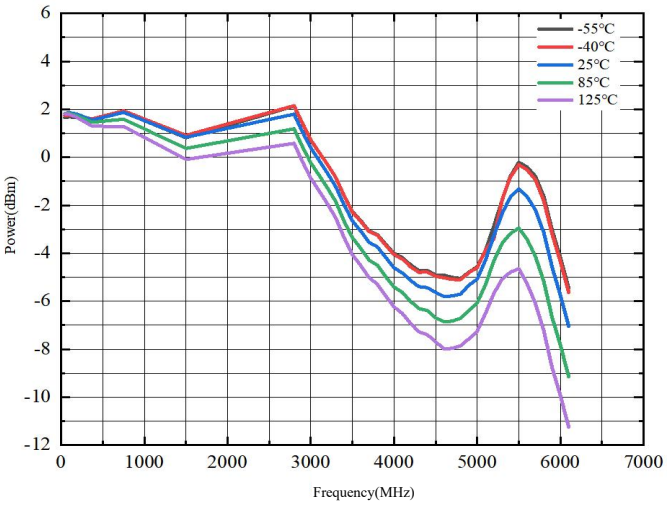


Figure 9. RFOUT+/- RF output medium-power mode

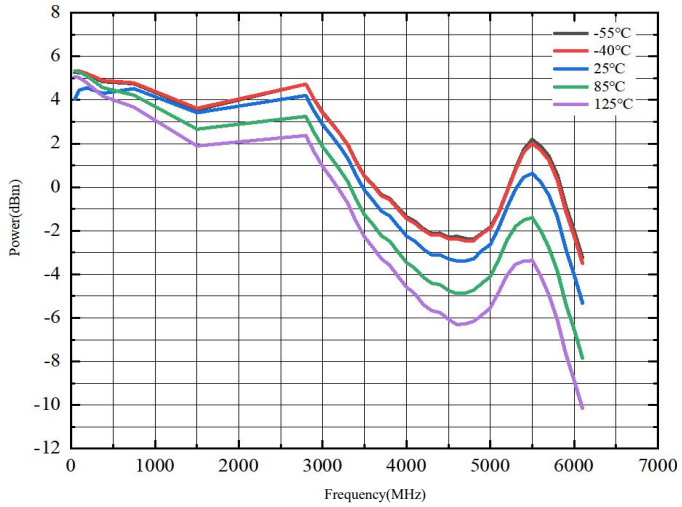
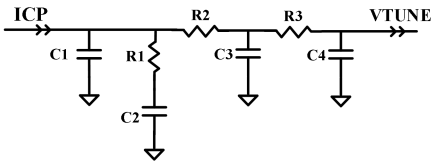
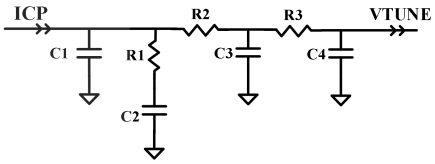


Figure 10. RFOUT+/- RF output high-power mode

Table 3. Loop Filter Design Reference

20MHz Phase Detection Frequency									
Loop Filter Number	Loop Filter Bandwidth(KHz)	C1 (nF)	R1 (Ω)	C2 (nF)	R2 (Ω)	C3 (nF)	R3 (Ω)	C4 (nF)	Loop Filter Design Reference Diagram
1	40	0.18	3600	3.3	2200	0.120	12000	0.038	
2	60	0.08	5340	1.5	3300	0.052	18000	0.018	
3（Recommended）	80	0.045	7130	0.820	4300	0.029	24000	0.009	
4	100	0.029	9100	0.526	5600	0.018	30000	0.006	
50MHz Phase Detection Frequency（Recommended）									
Loop Filter Number	Loop Filter Bandwidth(KHz)	C1 (nF)	R1 (Ω)	C2 (nF)	R2 (Ω)	C3 (nF)	R3 (Ω)	C4 (nF)	Loop Filter Design Reference Diagram
1	40	0.47	1391	8.6	910	0.297	4700	0.1	
2	60	0.2	2091	3.77	1300	0.135	7500	0.043	
3（Recommended）	80	0.115	2790	2.13	1800	0.076	10000	0.024	
4	100	0.076	3480	1.35	2200	0.047	12000	0.015	

Note: It is recommended that the loop filter be designed with a phase detection frequency of 50MHz and an ICP current of 400uA. Both integer and fractional performance are better compared to a phase detection frequency of 20MHz.

Pin functions

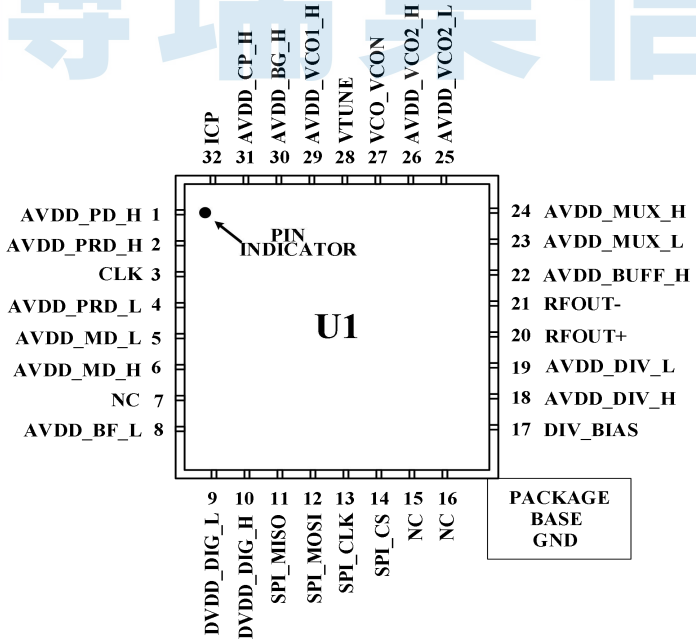


Figure 11. Pin Distribution

Table 4 Pin Description

Pin Number	Function	Description
1	AVDD_PD_H	Analog power 3.3V
2	AVDD_PRD_H	Analog power 3.3V
3	CLK	Reference clock input with external DC-blocking capacitor
4	AVDD_PRD_L	Analog power 1.2V
5	AVDD_MD_L	Analog power 1.2V
6	AVDD_MD_H	Analog power 3.3V
7	NC	No Connect
8	AVDD_BF_L	Analog power 1.2V
9	DVDD_DIG_L	Digital power 1.2V
10	DVDD_DIG_H	Digital power 3.3V
11	SPI_MISO	Multiplexer output, which can access lock detection, prescaled reference clock, N-divided feedback clock, and SPI read mode
12	SPI_MOSI	Serial communication data line (chip input)
13	SPI_CLK	Serial communication clock line
14	SPI_CS	Serial communication chip select line
15	NC	No Connect
16	NC	No Connect
17	DIV_BIAS	Internal bias port, externally connected to a grounded decoupling capacitor.
18	AVDD_DIV_H	Analog power 3.3V
19	AVDD_DIV_L	Analog power 1.2V
20	RFOUT+	Radio Frequency Output Port
21	RFOUT-	Complementary Radio Frequency Output Port
22	AVDD_BUFF_H	Analog power 3.3V
23	AVDD_MUX_L	Analog power 1.2V
24	AVDD_MUX_H	Analog power 3.3V
25	AVDD_VCO2_L	Analog power 1.2V
26	AVDD_VCO2_H	Analog power 3.3V
27	VCO_VCON	Internal bias port, externally connected to a 4.7uF grounded decoupling capacitor.
28	VTUNE	VCO control voltage, externally connected to the VTUNE port of the loop filter output
29	AVDD_VCO1_H	Analog power 3.3V
30	AVDD_BG_H	Analog power 3.3V
31	AVDD_CP_H	Analog power 3.3V
32	ICP	Charge pump output. This pin provides ±Icp to the external loop filter and is connected to the ICP port of the external loop filter.

Register Description

R/W(Read/Write)
R (Read - only)

REG0

R/W	CONTROL BITS																													
ADDRESS BITS	WR	PFD_DLY	I_OFFSETN_EN	I_OFFSETP_EN	ICP				I_OFFSET					SPI_OR_AFC	EN_CP	FK_SW	INT11B_R1													
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0/1	A1	A0	B0	0	C3	C2	C1	C0	D4	D3	D2	D1	D0	E0	F0	G0	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

DB27	R/W
0	W(default)
1	R

DB23	I_OFFSETP_EN
0	default

DB11	FK Enable
0	default

DB26	DB25	delay control
0	0	default

DB24	Enable Optimization of Boundary Spurious Signals
0	Close
1	Enable (Optimize Boundary Spurious)

DB18	DB17	DB16	DB15	DB14	Compensation Current Bit
0	0	0	0	0	0
0	0	0	0	1	1 (Recommended)
0	0	0	1	0	2
0	0	0	1	1	3
•	•	•	•	•	•
1	1	1	1	1	31

DB22	DB21	DB20	DB19	CP Current
0	0	0	1	400uA(Recommended)
0	0	1	0	800uA
0	0	1	1	1200uA
0	1	0	0	1600uA
•	•	•	•	• •
1	0	0	0	3200uA
•	•	•	•	• •
1	1	1	1	6000uA

DB13	AFC_OR_SPI
0	SPI Configuration Sub - band
1	AFC Configuration Sub-band (default)

DB12	Charge Pump Enable
0	CP Shutdown
1	CP Operation (Default)

DB10	DB9	• • •	DB4	DB3	DB2	DB1	DB0	
0	0	• • • •	0	0	0	0	0	NOT ALLOWED
•	•	• • • •	•	•	•	•	•	• • •
0	0	• • • •	0	0	0	0	0	NOT ALLOWED
0	0	• • • •	1	0	1	1	0	54
0	0	• • • •	1	0	1	1	1	55
0	0	• • • •	1	1	0	0	0	56
•	•	• • • •	•	•	•	•	•	• • •
•	•	• • • •	•	•	•	•	•	• • •
1	1	• • • •	1	1	1	1	1	2047

INTmin = 54 with Prescaler=4/5

Figure 12. Configuration Information of reg0 Register

REG1

R/W	CONTROL BITS																													
ADDRESS BITS	WR	CONRT3B			FRAC24B_R1																									
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0/1	M1	M0	0/1	FR23	FR22	FR21	FR20	FR19	FR18	FR17	FR16	FR15	FR14	FR13	FR12	FR11	FR10	FR9	FR8	FR7	FR6	FR5	FR4	FR3	FR2	FR1	FR0

Note: FRAC24B_R1=FRAC

DB27	R/W
0	W(default)
1	R

DB24	CONRT3B
0	SDM Shutdown
1	SDM On (Default)

DB26	DB25	SDM Mode
0	0	Traditional SDM (Default)
1	0	Scrambled SDM

DB23	DB22	• • • •	DB3	DB2	DB1	DB0	FRAC24B_R1
0	0	• • • •	0	0	0	0	0
0	0	• • • •	0	0	0	1	1
0	0	• • • •	0	0	1	0	2
0	0	• • • •	0	0	1	1	3
•	•	• • • •	•	•	•	•	• • •
•	•	• • • •	•	•	•	•	• • •
1	1	• • • •	1	1	0	0	16777212
1	1	• • • •	1	1	0	1	16777213
1	1	• • • •	1	1	1	0	16777214
1	1	• • • •	1	1	1	1	16777215

Figure 13. Configuration Information of reg1 Register

REG8

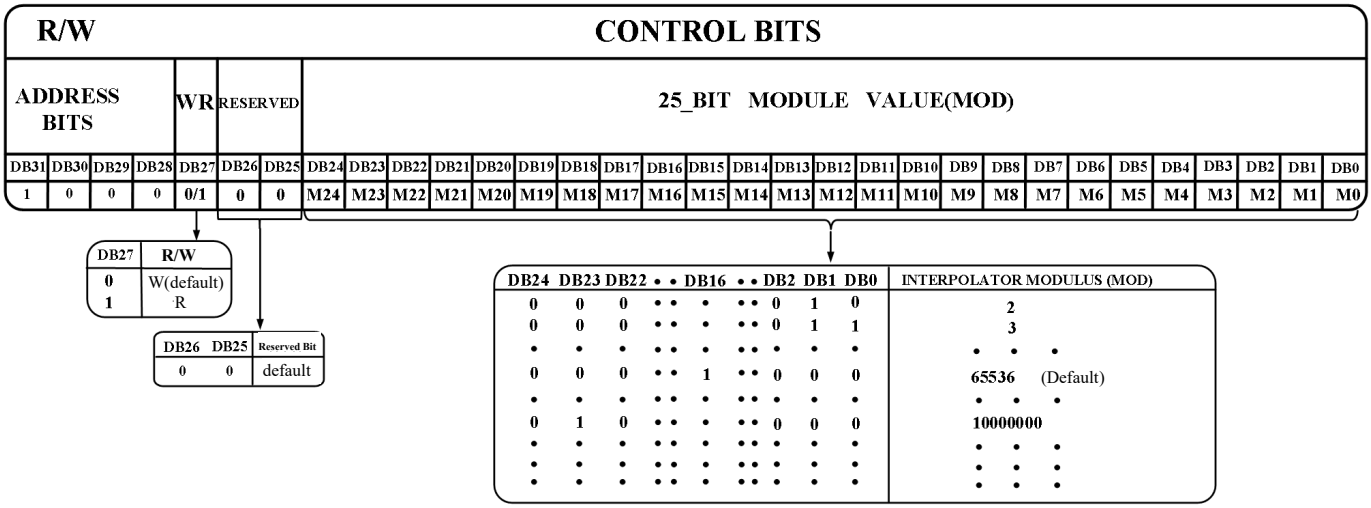


Figure 14. Configuration Information of reg8 Register

R/W(Read/Write)
R (Read - only)

REG9

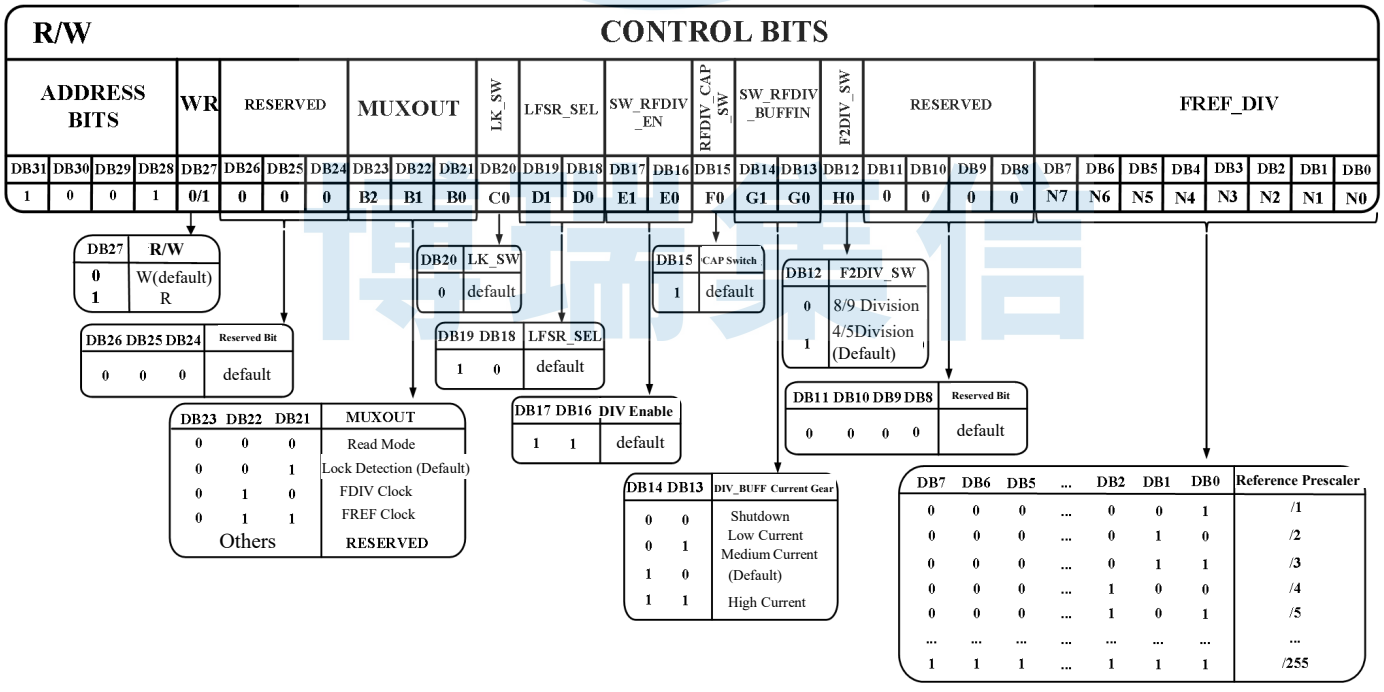


Figure 15. Configuration Information of reg9 Register

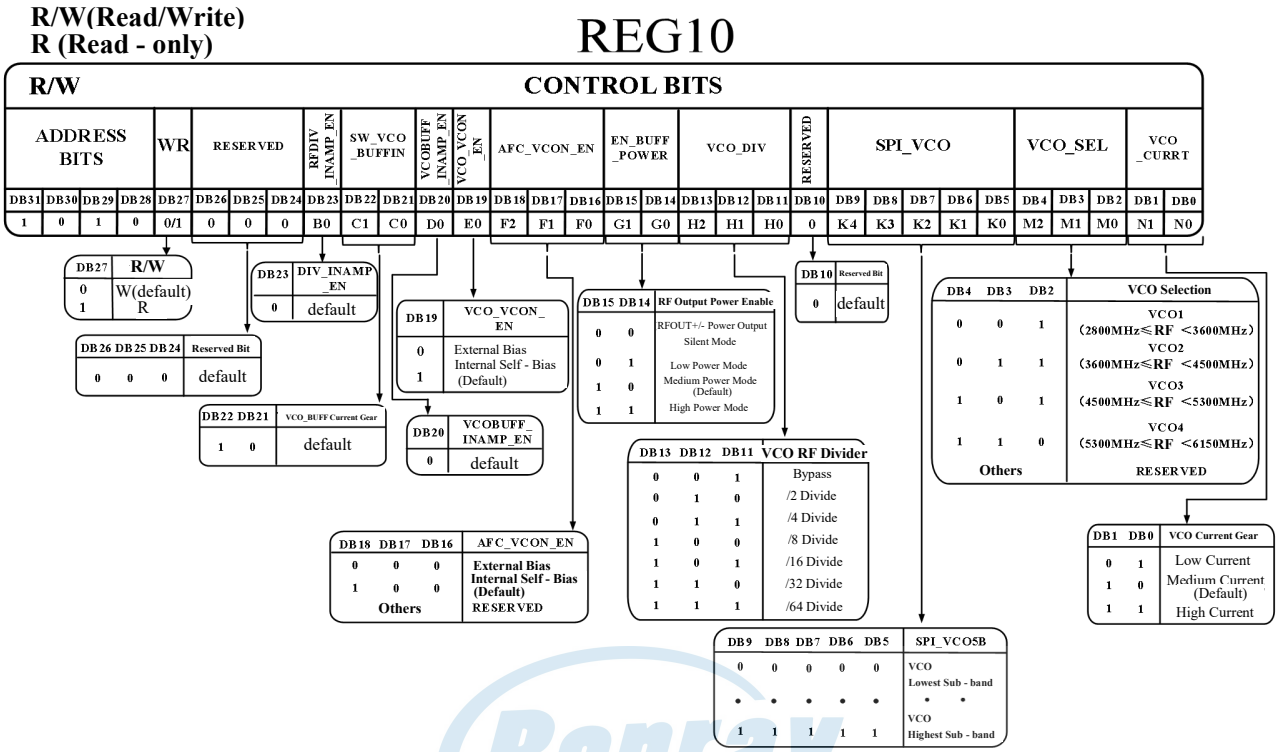


Figure 16. Configuration Information of reg10 Register

Register 0

Address bit

When the address bits DB[31:28] of Register 0 are 4'b0000, Register 0 can be programmed.

Read-write bit

When the read-write bit DB[27] of Register 0 is 1'b0, the write operation can be performed on Register 0.

OFFSET current enable bit

The OFFSET current enable bit DB[24] in Register 0 is used to optimize integer boundary spurs. When the boundary spurs of fractional frequency points fall within the passband and are difficult to suppress through the loop filter, the boundary spurs can be optimized by setting DB[24] = 1' b1. However, this will introduce current noise, degrading phase noise performance and reference spur performance. DB[24] in Register 0 needs to be used in conjunction with the I_OFFSET current DB[18:14] in Register 0. When using integer frequency points, DB[24] = 1'b0.

Charge pump current setting bits

The charge pump current setting bits DB[22:19] of Register 0 are used to set the charge pump current. The minimum charge pump current is 400uA with a step of 400uA, and the maximum current can reach 6mA. The loop bandwidth can be changed by appropriately adjusting the ICP current to balance the performance of integer and fractional frequency points. However, increasing the ICP current will deteriorate the reference spur performance.

SPI or AFC selection setting bit

The SPI or AFC selection setting bit DB[13] of Register 0 is used to select either automatic VCO sub-band selection or SPI-configured sub-band selection. When DB[13] = 1'b1, the VCO sub-band corresponding to the RF output frequency is automatically selected via the AFC

(Automatic Frequency Calibration) function. When DB[13] = 1'b0, the VCO sub-band corresponding to the RF output frequency is manually configured via SPI, and this function needs to be used in conjunction with the 5-bit VCO sub-band control bits SPI_VCO DB[9:5] of Register 10. Using the SPI-configured sub-band selection mode can effectively improve the locking time, and this mode should be used according to the VCO sub-band lookup table.

Charge pump enable bit

The charge pump enable bit DB[12] of Register 0 is used to control the on/off of the charge pump current. By default, the charge pump current is on with DB[27] = 1'b1.

INT value setting bit

The INT value setting bits DB[10:0] of Register 0 are used to set the INT value, which determines the integer part of the feedback division ratio. It is used in the formula:RF_{OUT}=[*INT*+(*FRAC*/*MOD*)]×[f_{PFD}]/*RF*Divider。Among them,RF_{OUT} is the radio frequency output frequency, *INT* is the integer part of the feedback division coefficient, *FRAC*/*MOD* is the fractional part of the feedback division coefficient,f_{PFD} is the phase - detection frequency, and the *RF* frequency divider is a VCO radio frequency frequency divider with a division ratio ranging from 1 to 64.

Register 1

Address bit

When the address bits DB[31:28] of Register 1 are 4'b0001, Register 1 can be programmed.

Read - write bit

When the read-write bit DB[27] of Register 1 is 1'b0, the write operation can be performed on Register 1.

SDM mode and switch setting bits

The SDM mode and switch setting bits DB[26:24] of Register 1 are used to set the SDM mode and switch. When the SDM mode and switch DB[26:24] = 3'b001, the SDM works in traditional mode to implement the fractional function.

FRAC setting bits

The FRAC setting bits DB[23:0] of Register 1 are used to set the numerator value of the SDM fractional input. It is used in conjunction with the denominator MOD value of the SDM fractional input to implement the fractional part of the feedback division ratio.

Register 8

Address bit

When the address bits DB[31:28] of Register 8 are 4'b1000, Register 8 can be programmed.

Read-write bit

When the read-write bit DB[27] of Register 8 is 1'b0, the write operation can be performed on Register 8.

MOD modulus setting bits

The MOD modulus setting bits DB[24:0] of Register 8 are used to set the denominator modulus value of the SDM fractional input. It is used in conjunction with the numerator FRAC value of the SDM fractional input to implement the fractional part of the feedback division ratio. The default setting of the MOD modulus bits DB[24:0] is 25'd65536.

Register 9

Address bit

When the address bits DB[31:28] of Register 9 are 4'b1001, Register 9 can be programmed.

Read-write bit

When the read-write bit DB[27] of Register 9 is 1'b0, the write operation can be performed on Register 9.

MUXOUT setting bits

The MUXOUT setting bits DB[23:21] of Register 9 are used to access functions such as lock detection, prescaled reference clock, N-divided feedback clock, and SPI reading, with lock detection being the default access.

Dual-mode prescaler setting bits

The dual-mode prescaler setting bit DB[12] of Register 9 is used to set 4/5 division or 8/9 division. Since the maximum RF frequency allowed by the dual-mode prescaler based on synchronous 4/5 division meets the highest frequency, the full frequency band is set to 4/5 division by default.

Reference prescaler setting bits

The reference prescaler setting bits DB[7:0] of Register 9 are used to prescale the input reference clock frequency (REFIN) to meet the input frequency range of the phase detector. A division ratio range of 1 to 255 can be achieved.

Register 10

Address bit

When the address bits DB[31:28] of Register 10 are 4'b1010, Register 10 can be programmed.

Read-write bit

When the read-write bit DB[27] of Register 10 is 1'b0, the write operation can be performed on Register 10.

RFOUT+/- RF output power mode setting bits

The RF output power mode setting bits DB[15:14] of Register 10 are used for the output and mute of RFOUT+/- RF power. When DB[15:14] = 00, it is the RF output mute mode, and the power of the mute output lock signal is ≤ -50dBm; when DB[15:14] = 01, it is the RF power low-power output mode; when DB[15:14] = 10, it is the RF power medium-power output mode; when DB[15:14] = 11, it is the RF power high-power output mode.

VCO RF frequency divider setting bits

The VCO RF frequency divider setting bits DB[13:11] of Register 10 are used to divide the RF output frequency by a factor of 1 to 64, so as to expand the frequency band range. For specific configurations, please refer to the configuration information of Register 10.

VCO sub-band 5-bit control bits

The 5-bit VCO sub-band control bits DB[9:5] of Register 10 are used to select 32 different sub-bands of the VCO. This function needs to be used in conjunction with the SPI_OR_AFC selection setting bit of DB[13] in Register 0. When DB[13] of SPI_OR_AFC is 0, the 5-bit VCO sub-band control bits are valid.

VCO selection setting bits

The VCO selection setting bits DB[4:2] of Register 10 are used to select VCOs for output of different RF frequency bands. When DB[4:2] = 3'b001, VCO1 with RF output frequency in the range of 2800MHz ≤ RF output frequency < 3600MHz is selected; when DB[4:2] = 3'b011,

VCO2 with RF output frequency in the range of 3600MHz ≤ RF output frequency < 4500MHz is selected; when DB[4:2] = 3'b101, VCO3 with RF output frequency in the range of 4500MHz ≤ RF output frequency < 5300MHz is selected; when DB[4:2] = 3'b110, VCO4 with RF output frequency in the range of 5300MHz ≤ RF output frequency < 6150MHz is selected.

Configuration sequence of Registers 0 to 10

After 1uF, 0.1uF, and 0.01uF capacitors are placed in sequence at the power supply pin to maximize the filtering of interference on the power line and ensure normal power-up,

BR9069FLJ completes the configuration in the following register sequence:

Register 10 → Register 9 → Register 8 → Register 1 → Register 0; Registers 2 to 7 are invalid and do not need to be configured. If frequency hopping from 3000MHz to 3011MHz is required, only FRAC24B_R1 in Register 1 and INT11B_R1 in Register 0 need to be changed, and Register 1 → Register 0 should be resent.

Frequency point configuration description

The following uses an application case to illustrate how to configure:

$RF_{OUT}=[INT+(FRAC/MOD)]\times[f_{PFD}]/RF\ divider$

Among them, RF_{OUT} is the RF output frequency, INT is the integer division coefficient, FRAC is the fractional division coefficient, MOD is the modulus, f_{PFD} is the phase detector frequency, and the RF divider is the RF output division number of the VCO.

$f_{PFD} = REFIN \times [1/R]$ where REFIN is the reference frequency input and R is the reference prescaling coefficient.

Suppose the existing RF system needs an output frequency (RF_{OUT}) of 3000.2MHz, the frequency of the reference crystal oscillator (REFIN) is 20MHz, and the frequency channel resolution (f_{RESOUT}) is 200KHz. Thus:

The VCO output frequency of BR9069FLJ is 3000 - 6000MHz, so the RF divider = 1; the output requirement of the RF divider is a 200KHz channel resolution (f_{RESOUT}), so the channel resolution of the VCO output is also 200KHz (f_{RES}).

MOD =65536

$f_{PFD} = 20MHz \times [(1)/(1)]=20MHz$

$3000.2=20\times[INT+(\frac{FRAC}{65536})]$

It can be obtained that: INT =150

FRAC=655

In the above calculation, the MOD value is 65536. And when calculating f_{PFD}, the reference division factor R is set to 1. The value of f_{PFD} here can be flexibly set, but it should be less than or equal to the maximum phase - detection frequency of the PFD.

Application Information

Figure 17 shows the typical application circuit of BR9069FLJ. The chip is powered by 3.3V and 1.2V power supplies, and it is recommended to use an LDO for chip power supply. The noise performance of the LDO will reduce its impact on the noise performance of BR9069FLJ. The chip requires an external loop

filter to work, and a 4th-order loop filter is recommended. The input reference signal needs to be provided by an external crystal oscillator.

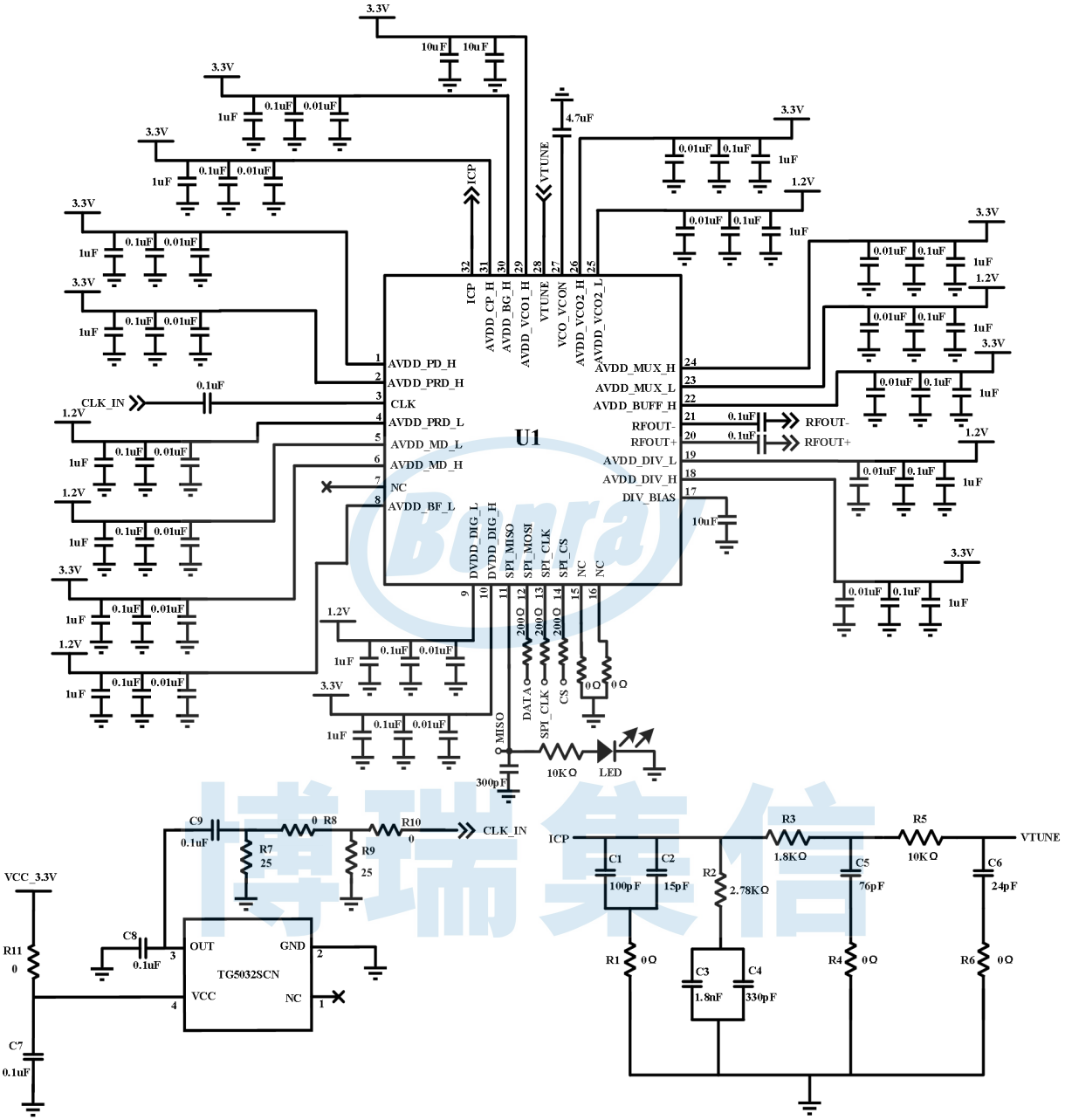
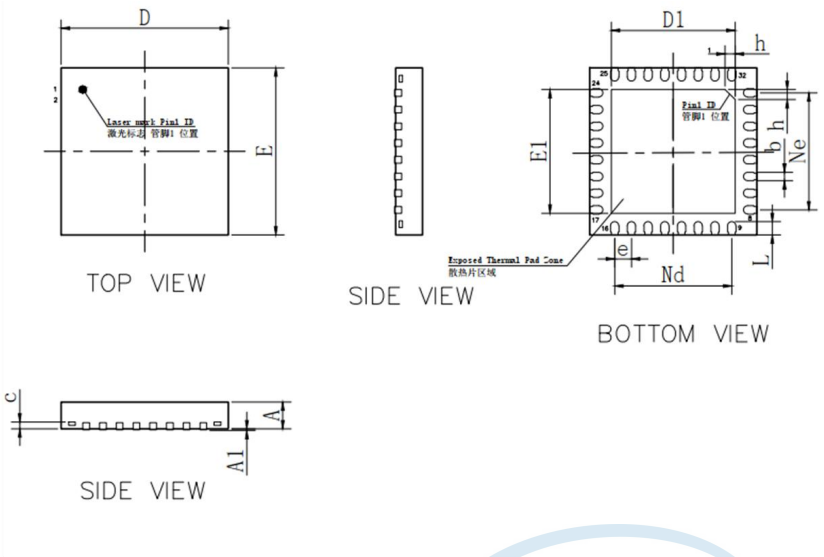


Figure 17. Typical Application Circuit

Package Information (Unit: mm)



SYMBOL 符 号	MILLIMETER		
	MIN 最小	NOM 标称	MAX 最大
A	0.75	0.80	0.85
A1	--	0.02	0.05
b	0.20	0.25	0.30
c		0.203REF	
D	4.90	5.00	5.10
D1	3.35	3.40	3.45
e		0.50BSC	
Ne		3.50BSC	
Nd		3.50BSC	
E	4.90	5.00	5.10
E1	3.35	3.40	3.45
L	0.35	0.40	0.45
h	0.25	0.30	0.35

Figure 18. Package Information Diagram