Product Features

Frequency：2.7GHz～3.1GHz

Psat：55dBm@3GHz

PAE：59%@3GHz

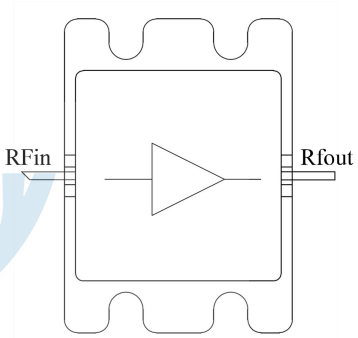
VDD Supply Voltage 50V, IDQ 600mA

Package: PJ (metal package)

General Description

BRGF031300PJG is an internally matched power amplifier that operates in the frequency range of 2.7GHz to 3.1GHz. This product is powered by a +50V drain supply voltage, delivering a saturated output power of 300W with excellent efficiency. It is suitable for specialized communication and radar applications.

Functional Block Diagram



Applications

Jammers

Radar

Ordering Information

Part Number	Package	Description
BRGF031300PJG	PJ	2.7GHz~3.1GHz 300W internally matched PA

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	150V
Gate Voltage Range (V_{GG})	-10~2V
Drain current（ID）	56mA
Mounting temperature	300℃，＜30s
Storage temperature	-65℃～+150℃

Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and. exposure to absolute-maximum ratings conditions for extended periods will affect the reliability. Under high temperature operation, please pay attention to good Dissipate heat.

Recommended Operating Conditions

Parameters	Values
Drain voltage（VDD）	+50V（Typ）
Drain static current（IDQ）	100mA（Typ）
Gate voltage（VGG）	-3.3V（Typ）
Channel temperature（TCH）	＜225℃
Continuous dissipated power（PD）	＜260W
Operating temperature	-55℃～+85℃

Note: The power amplifier transistor electrical specifications are tested under the specified Test Condition. Electrical performance is not guaranteed when the test specifications are exceeded.

Thermal Parameters

Parameters	Test Condition	value	Units
$R_{\theta jc}$	Dc bias Test at 85° C	0.75	℃/W

Note: $R_{\theta jc}$ to measure the thermal resistance to the bottom of the package;

ESD WARNING

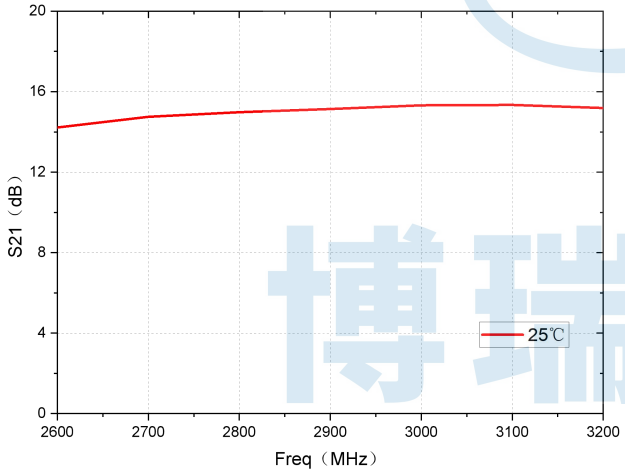
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Typical Performance（EVB test data，2.7GHz~3.1GHz）

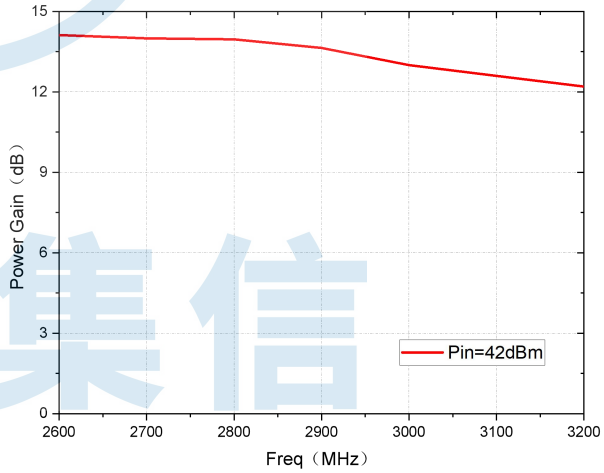
Parameters	Typ.						Units
Frequency	2.6	2.7	2.8	2.9	3.0	3.1	GHz
S21	14.2	14.8	15	15.1	15.3	15.3	dB
S11	-3	-3.3	-3.5	-3.8	-4.1	-4.6	dB
P_{sat}	55.8	55.7	55.5	55	55	54.2	dBm
PAE@P_{sat}	52	56	58	57	59	56	%
Gain@P_{sat}	14	14	13.9	13.6	13	12.6	dB
2^{nd} Harmonic@P_{sat}	37.2	44.7	47.9	55.6	55	57.6	dBc
3rd Harmonic@P_{sat}	32.9	32.8	31.9	31.8	31.5	30.9	dBc
Test condition：At Temp = +25°C, small-signal testing is conducted at +50V and 600mA. The output saturation power test employs a pulsed signal with a period of 1ms and a pulse width of 100μs, with a quiescent current of 0mA and an input power of 42dBm.							

Note:P_{sat} defined as the saturation power output of the evaluation board.;

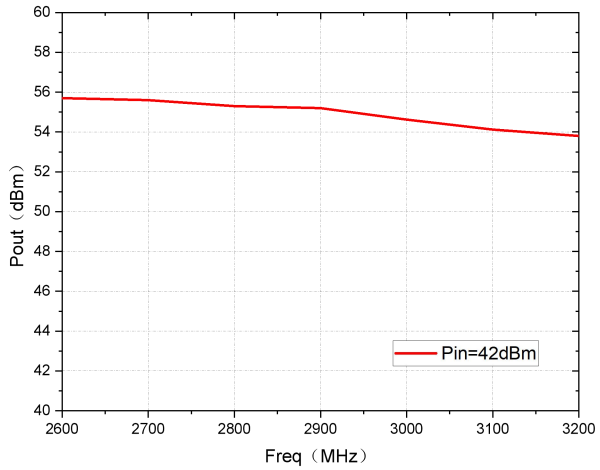
Typical Performance Plots（EVB test data）



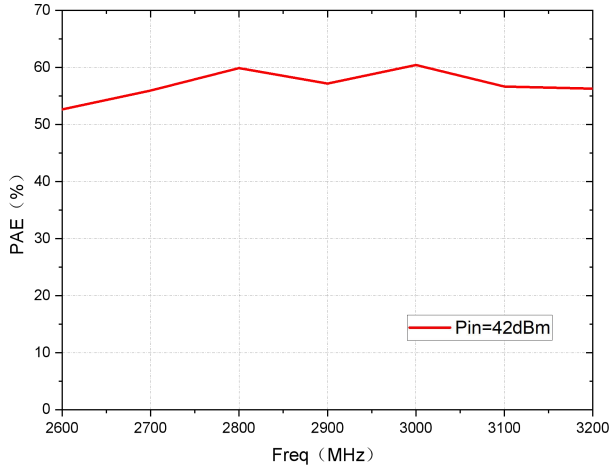
S21



Power Gain

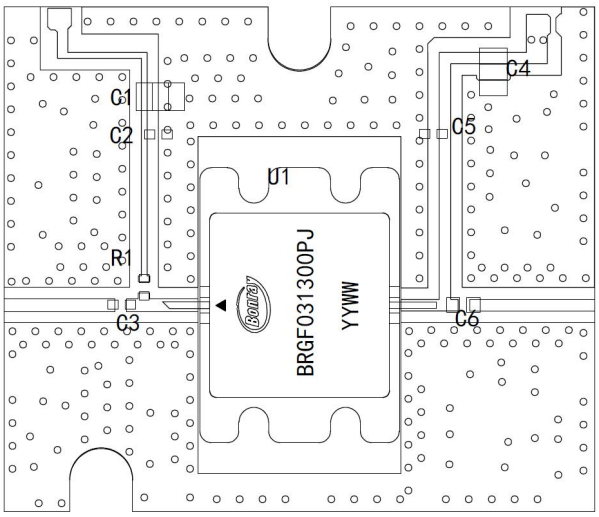


Psat



PAE

PCB Evaluation Board



Bill of Material

Designator	Package	Description	Part Number
C1	1210	10uF	GRM32EC72A106KE05#
C4	1210	10 uF *5	GRM32EC72A106KE05#
U1	PJ	BRGF031300PJG	BRGF031300PJG
R1	0603	30ohm	/
C2	0603	6 pF	GQM1875G2E6R0BB12
C3,C6	0603	7.9pF	GQM1875G2E7R9BB12
C5	0603	10pF	GQM1875C2E100FB12#

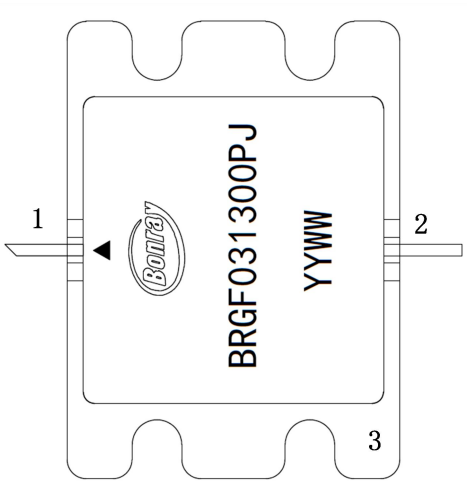
1.To ensure optimal heat dissipation and grounding performance, it is recommended to solder and secure the bottom of the device to an external heat dissipation structure.

2.If soldering the bottom is not feasible, the device should be installed using screws with anti-loosening measures. Additionally, indium foil must be placed under the device to ensure effective grounding and heat dissipation.

3.The slot design on the printed circuit board (PCB) and metal structural components should be optimized to ensure the device leads are positioned 0.1mm above the PCB surface.

4.The device must be centered within the slot, with the distance between its input/output end faces and the edges of the PCB slot maintained within the range of 0.1–0.15mm.

Pin Configuration



Description

Pin Number	Pin Name	Description
1	V_{GG}/ RFin	Gate voltage / RF Input matched to 50 ohms;
2	V_{DD} / RFout	Drain voltage / RF Output matched to 50 ohms;
3	Package Base	Source connected to ground;

Power-on Sequence

1.Set the gate voltage (Vg) to -5V and enable the gate voltage supply.

2.Set the drain voltage (Vd) to +50V, enable the drain voltage supply, and adjust the gate voltage to achieve a drain current (Id) of 600mA.

3.Apply the RF input signal.

Power-off Sequence

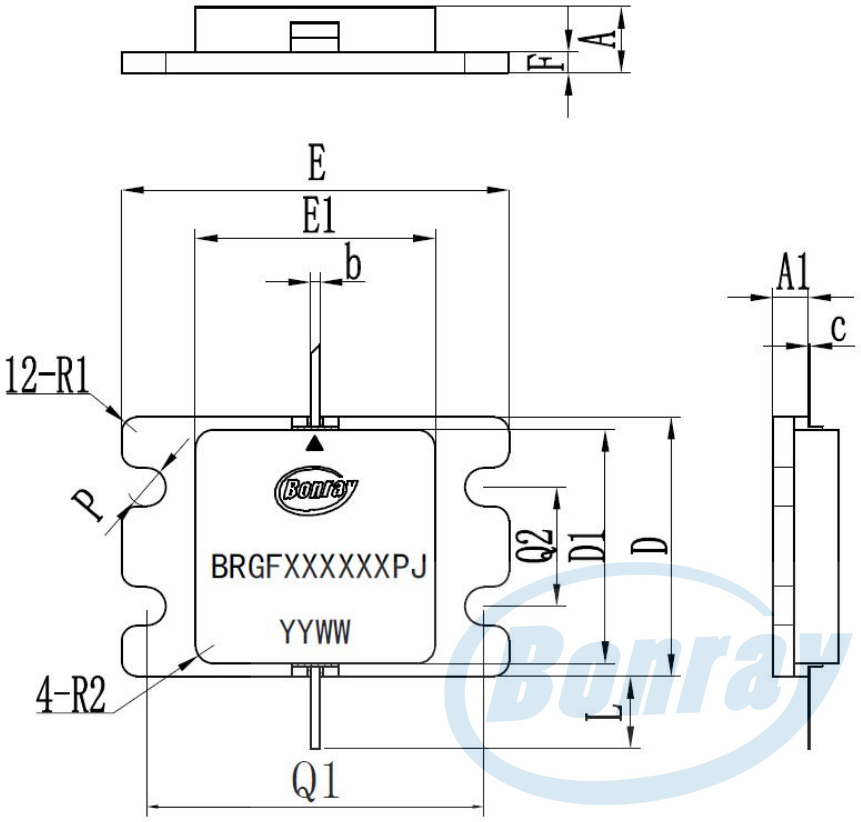
1.Turn off the RF input signal.

2.Disable the drain voltage supply and wait for 5 seconds to allow complete discharge of the drain capacitance.

3.Turn off the gate bias voltage.

Note: When the circuit is designed, a timing protection circuit is required to power off the V_{GG} Ensure that the V_{DD} is added after the V_{GG} is fully powered on. Ensure that the V_{DD} is lower than 5V before powering off the V_{GG}.Especially in T_{DD} applications, grid-supplied decoupling capacitors need to be rigorously evaluated to meet switching speed requirements.

Package Dimensions (Units:mm)



尺寸项	单位：mm		
	最小值	典型值	最大值
A	4.25	4.5	4.75
A1	2.25	2.4	2.55
b	0.55	0.6	0.65
c	0.05	0.1	0.15
D	17.25	17.4	17.55
D1	15.55	15.7	15.85
E	23.85	24	24.15
E1	15.95	16.1	16.25
F	1.3	1.4	1.5
L	3.2	3.5	3.8
P	-	2.6	-
Q1	20.25	20.4	2.65
Q2	7.9	8	8.1
R1	-	1	-
R2	-	1.25	-

Recommended Soldering Temperature Profile