## Product Features

Frequency：DC～3.0GHz

S21：18.1dB@1.2GHz

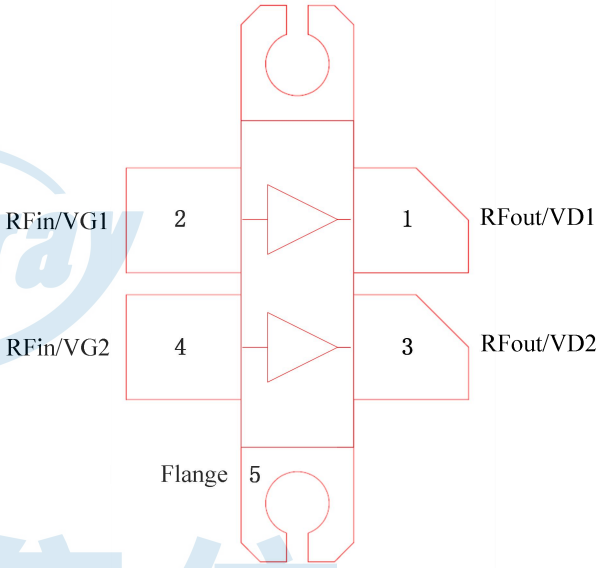
Psat：51.5dBm@1.1GHz

PAE：59.2%@1.2GHz

Operation Voltage：28V, static current 800mA

Package：PF（ceramic seal）


## Functional Diagram




## General Description

The BRGM030150PF is a gallium nitride (GaN) pre-matched pair transistor with a +28V drain supply ， that delivers 150W(51.8dBm) of transistor output in a DC to 3.0GHz bandwidth with a power added efficiency (PAE) up to 59.2%.The product uses GaN process and has the characteristics of high efficiency, high gain and wide bandwidth, which makes the product has strong application capabilities in both linear and compressed amplifier circuits, while also simplifying link design and related heat consumption management.

## 应用

Wide Band Communications

Radar

Test instrumentation

Wideband or narrowband amplifiers

Jammers

## Ordering Information

| Part Number | Package | Description |
|---|---|---|
| BRGM030150PF | PF | DC～3.0GHz<br>150W dual path<br>transistor |

## Absolute Maximum Ratings

| Parameters | values |
|---|---|
| Gate drain breakdown voltage（$BV_{DG}$） | 100V |
| Gate Voltage Range（$V_{GG}$） | -6～0V |
| Drain current（$I_D$） | 15A |
| Gate current（$I_G$） | 38mA |
| Mounting temperature（30 seconds） | 245℃ |
| Storage temperature | -65℃～+150℃ |
| Operating temperature | -55℃～+85℃ |

Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and exposure to absolute-maximum ratings conditions for extended periods will affect the reliability. Under high temperature operation, please pay attention to good Dissipate heat.

## Recommended Operating Conditions

| Parameters | values |
|---|---|
| Drain voltage（$V_{DD}$） | +28V（Typ） |
| Drain static current（$I_{DQ}$） | 840mA（Typ） |
| Gate voltage（$V_{GG}$） | -2.7V（Typ） |
| Channel temperature（$T_{CH}$） | 225℃（Max） |
| Continuous dissipated power（$P_D$） | 128W（Max） |

Note: The power amplifier transistor electrical specifications are tested under the specified Test Condition. Electrical performance is not guaranteed when the test specifications are exceeded.

## Impedance Mismatch

| Symbol | Parameters | values |
|---|---|---|
| VSWR | Impedance Mismatch Ruggedness | 5:1 |

Test Condition: DEMO board test, TA=25℃, VDD=+28V, Freq=1.1GHz, CW wave, Pout=150W test;

## Thermal Parameters

| Parameters | Test Condition | value | Units |
|---|---|---|---|
| Thermal resistance（$\theta_{JC}$） | Dc bias Test at 70 ° C | 1.1 | ℃/W |
| Channel temperature（$T_{ch}$） | | 225 | ℃ |

Note: $\theta_{JC}$ to measure the thermal resistance to the bottom of the tube housing;

## ESD warning

**ELECTROSTATIC SENSITIVE DEVICE**

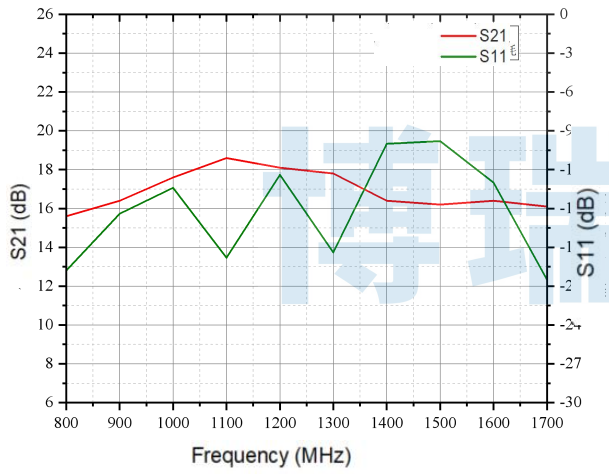
**OBSERVE HANDLING PRECAUTIONS**

## Typical Performance (EVB test data)

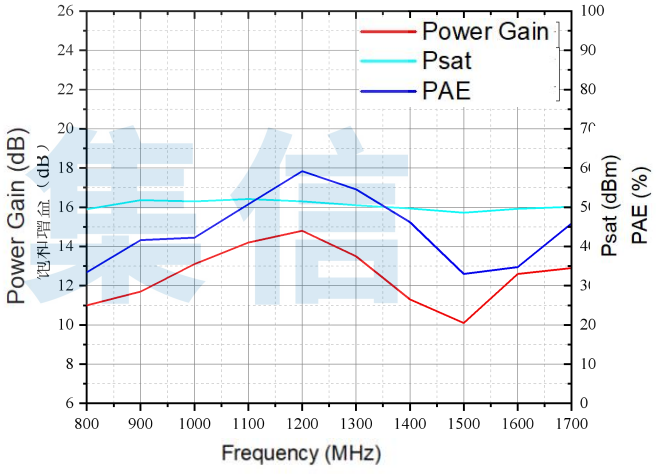
| Parameters | Typ. | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Frequency | 800 | 900 | 1000 | 1100 | 1200 | 1300 | 1400 | 1500 | 1600 | 1700 | MHz |
| S21 | 15.6 | 16.4 | 17.6 | 18.6 | 18.1 | 17.8 | 16.4 | 16.2 | 16.4 | 16.1 | dB |
| S11 | -19.8 | -15.4 | -13.4 | -18.8 | -12.4 | -18.4 | -10 | -9.8 | -13 | -20.5 | dB |
| Drain Current @$P_{sat}$ | 8.8 | 12.1 | 11.4 | 11.0 | 8.2 | 7.0 | 6.7 | 7.1 | 8.9 | 7.6 | A |
| $P_{sat}$ | 49.5 | 51.8 | 51.5 | 52.1 | 51.5 | 50.5 | 49.7 | 48.6 | 49.6 | 50.1 | dBm |
| PAE@$P_{sat}$ | 33.4 | 41.6 | 42.2 | 50.8 | 59.2 | 54.5 | 46.2 | 33.0 | 34.7 | 45.9 | % |
| Gain @$P_{sat}$ | 11 | 11.7 | 13.1 | 14.2 | 14.8 | 13.5 | 11.3 | 10.1 | 12.6 | 12.9 | dB |
| Test condition：Temp =+25℃，$V_{DD}$=+28V，$I_{DQ}$=800mA； | | | | | | | | | | | |

Note:$P_{sat}$ defined as the saturation power output of the evaluation board.

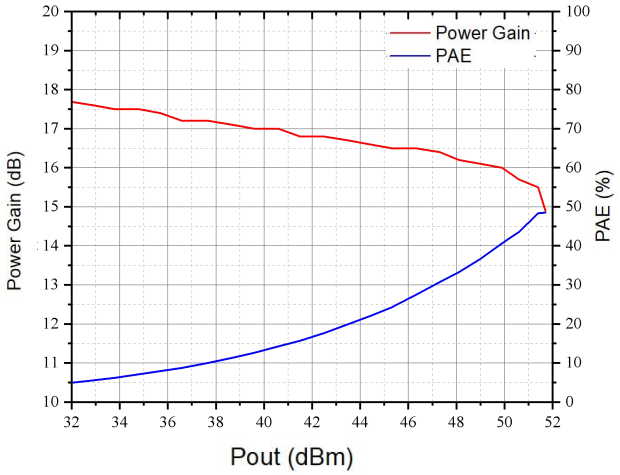
## Typical Performance（test on EVB 0.8GHz-1.7GHz，Temp =+25℃，$V_{DD}$=+28V，$I_{DQ}$=800mA）



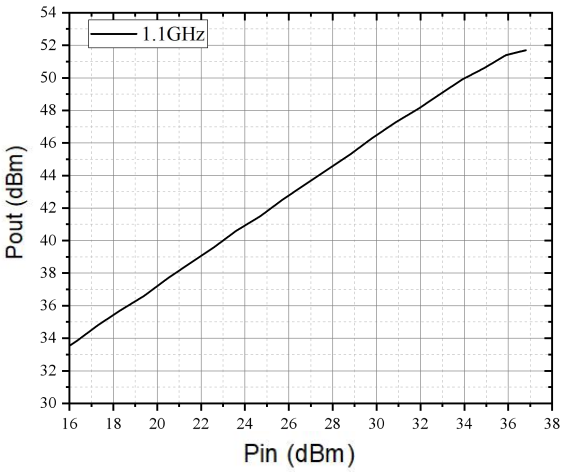

S21、S11 vs. Freq



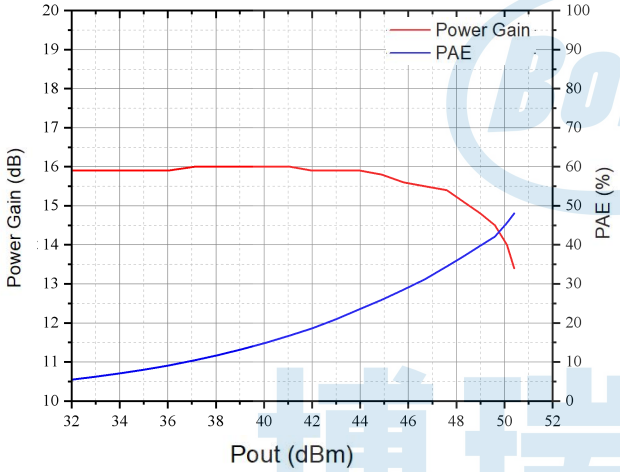

Gain、Psat、PAE vs.Freq



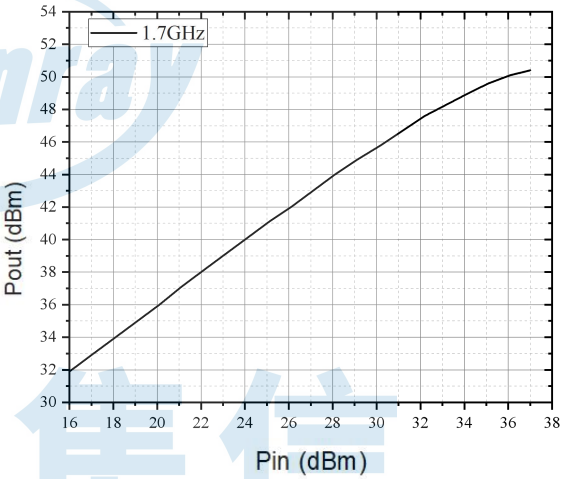

Gain、PAE vs.Pout（1.1GHz）




Pout vs.Pin（1.1GHz）

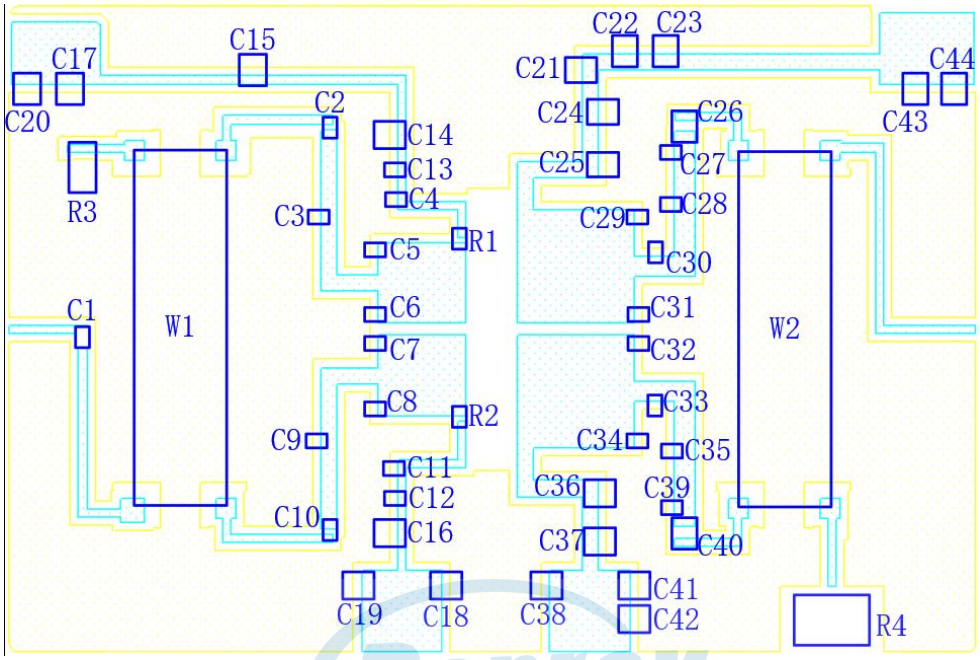



Gain、PAE vs.Pout




Pout vs.Pin（1.7GHz）

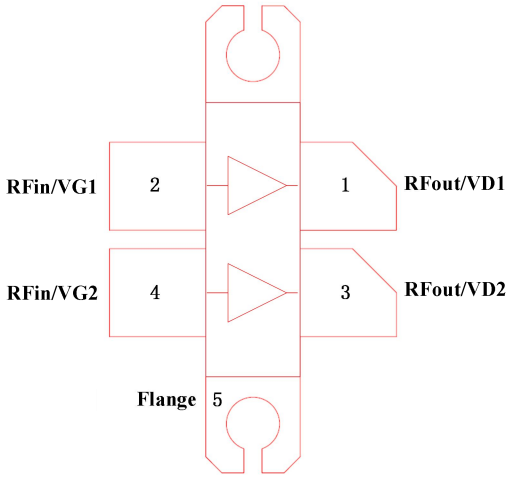
**PCB Evaluation Board**




## Bill of Material

| Designator | Description | Package | Qty |
|---|---|---|---|
| C1,C2,C4,C10,C11 | CAP,39pF,50VDC | C0603 | 5 |
| C3,C9 | CAP,1pF,50VDC | C0603 | 2 |
| C5~C8 | CAP,2.4pF,50VDC | C0603 | 4 |
| C29,C31,C32,C34 | CAP,1.8pF,250VDC | C0603 | 4 |
| C27,C30,C33,C39 | CAP,0.5pF, 250VDC | C0603 | 4 |
| C28,C35 | CAP,1.5pF,250VDC | C0603 | 2 |
| C25,C26,C36,C40 | CAP,39pF,250VDC | C1111 | 4 |
| C12,C13 | CAP,1000pF,50VDC | C0603 | 2 |
| C14~C20 | CAP,10uF,50VDC | C1210 | 7 |
| C21~C24,C37,C38,C41~C44 | CAP,10uF,250VDC | C1210 | 10 |
| R1,R2 | RES,49.9Ohm | R0603 | 2 |
| R3 | RES,50Ohm,20W | / | 1 |
| R4 | RES,50Ohm,150W | / | 1 |
| W1,W2 | 3dB combiner,150W | / | 2 |

## Pin Configuration and Description




| Pin Number | Pin Name | Description |
|---|---|---|
| 1/3 | RFout/$V_{DD}$ | Drain voltage / RF Output matched to 50 ohms; |
| 2/4 | RFin/$V_{GG}$ | Gate voltage / RF Input matched to 50 ohms; |
| - | Package Base | Source connected to ground; |

**Power-on Sequence**

1.Set the gate voltage ($V_{GG}$) to -5V;

2.Set drain voltage ($V_{DD}$) to +28V;

3. Turn on the gate voltage;

4. Turn on drain voltage;

5.Slowly increase VG until quiescent ID is 800 mA.

**Power-off Sequence**

1. Turn off the RF signal;

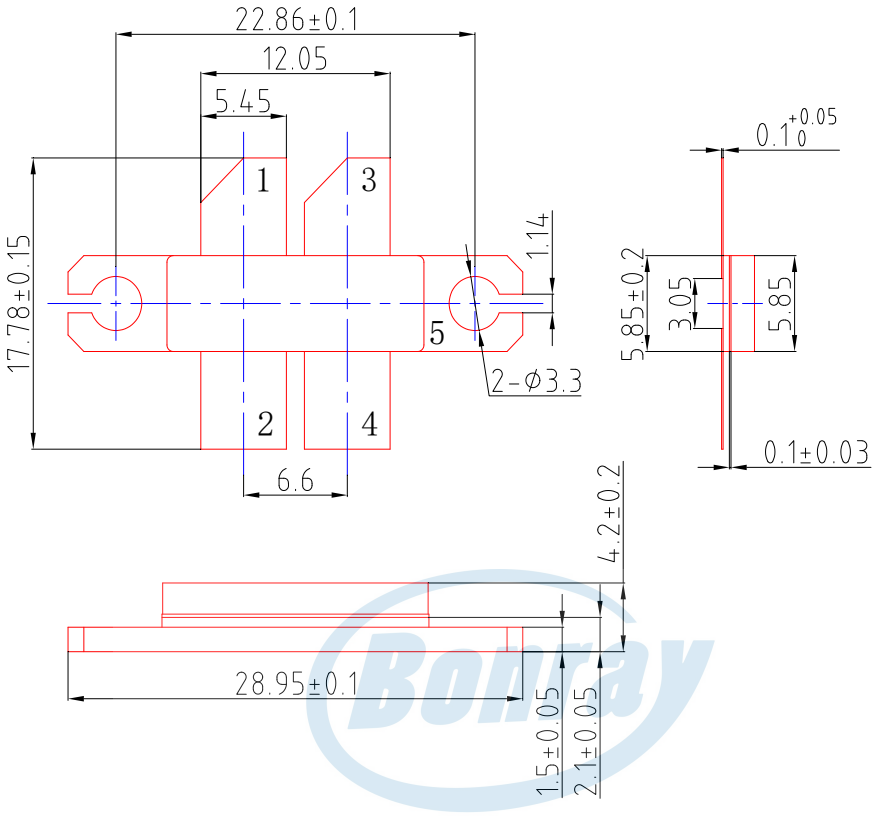
2. Reduce the gate voltage ($V_{GG}$) to -5V;

3. Turn off drain supply voltage;

4. Turn off the grid supply voltage;

Note: When the circuit is designed, a timing protection circuit is required to power off the $V_{GG}$. Ensure that the $V_{DD}$ is added after the $V_{GG}$ is fully powered on. Ensure that the $V_{DD}$ is lower than 5V before powering off the $V_{GG}$. Especially in $T_{DD}$ applications, grid-supplied decoupling capacitors need to be rigorously evaluated to meet switching speed requirements.

## Package Dimensions (Units:mm)




## Recommended Soldering Temperature Profile