Product Features

Frequency: 1.9GHz ~ 2.4GHz

Gain: 18.6dB@2.2GHz

Psat: 45.7dBm@2.2GHz

PAE: 59.5%@2.2GHz

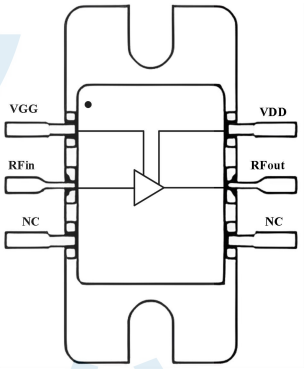
Operation Voltage: 28V, static current 200mA

Package: PH (metal package)

General Description

BRGF024025PHG is a Gallium nitride (GaN) internal matching power amplifier, the product covers the frequency range of 1.9GHz ~ 2.4GHz, using +28V drain power supply, static operating current 200mA. Thanks to the internal matching design, only the isolating capacitor and decoupling capacitor can be added to the outside during application, which is convenient for system application.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGF024025PHG	PH	1.9 GHz to 2.4 GHz 25W Internal Power Amplifier

Applications

Satellite Communications

Telemetry Equipment

Universal Transmitter

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain Current (I_D)	5A
Gate Current (I_G)	9mA
Continuous Dissipated Power (P_D)	50W
Channel Temperature (T_{CH})	275 ℃
Mounting Temperature (30 seconds)	245 ℃

Note: Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Values
Drain Voltage (V_{DD})	+28V (Typ)
Drain Static Current (I_{DQ})	200mA (Typ)
Gate Voltage (V_{GG})	-2.32V (Typ)
Channel Temperature (T_{CH})	225 ° C (25 ° C)
Storage Temperature	-65℃ ~ +150℃
Operating Temperature	-55℃ ~ +85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	10:1

Test Conditions: DEMO board test, T_A =25℃, V_{DD} =+28V, I_{DQ} =200mA, Freq=2GHz, CW wave, P_{out}=25W test;

Thermal Parameters

Parameters	Test Conditions	Value	Units
Thermal Resistance (θ_{JC})	Static bias condition, tested at 85 ° C	5	℃/W

Note: θ_{JC} to measure the thermal resistance to the bottom of the tube housing;

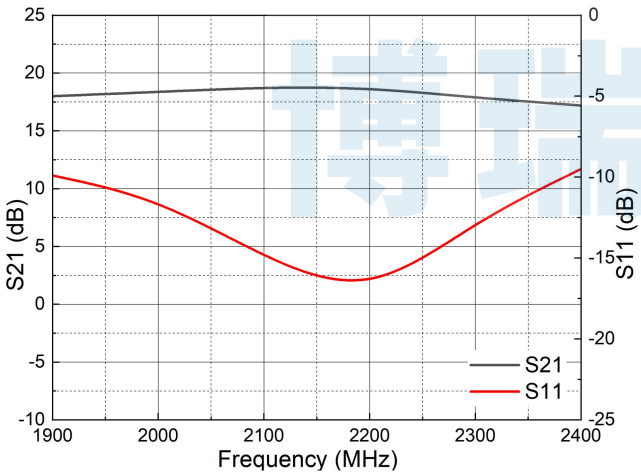
ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

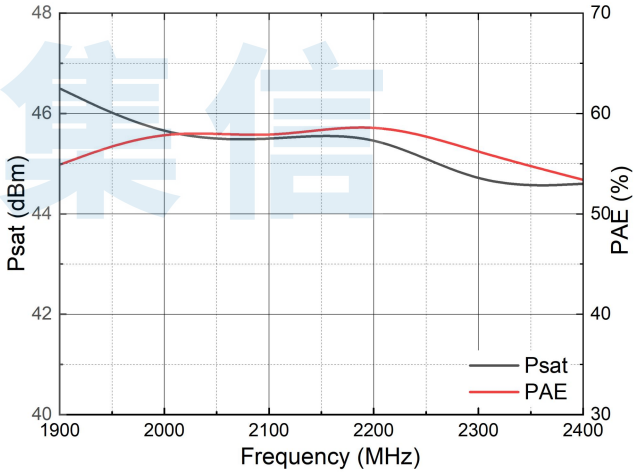
Typical Performance: EVB test data (1.9GHz ~ 2.4GHz)

Parameters	Typ.						Units
Frequency	1900	2000	2100	2200	2300	2400	MHz
Gain	18.0	18.37	18.7	18.6	17.9	17.2	dB
Input Return Loss	-9.9	-11.3	-15	-17.5	-12.7	-9.5	dB
Output Return Loss	-7.6	-9.6	-15.5	-23	-15	-11.5	dB
Pout (dBm) @P_{sat}	46.5	45.5	45.45	45.7	44.5	44.6	dBm
Drain Current @P_{sat}	2760	2074	2096	2139	1700	1830	mA
PAE@P_{sat}	54.9	58.7	57.3	59.5	56.1	53.4	%
Power Gain @P_{sat}	13.0	14.0	13.8	13.9	12.8	12.9	dB
Test Condition: Temp =+25 ° C, V_{DD}=+28V, I_{DQ}=200mA Note: P_{sat} defined as the Psat output of the evaluation board.							

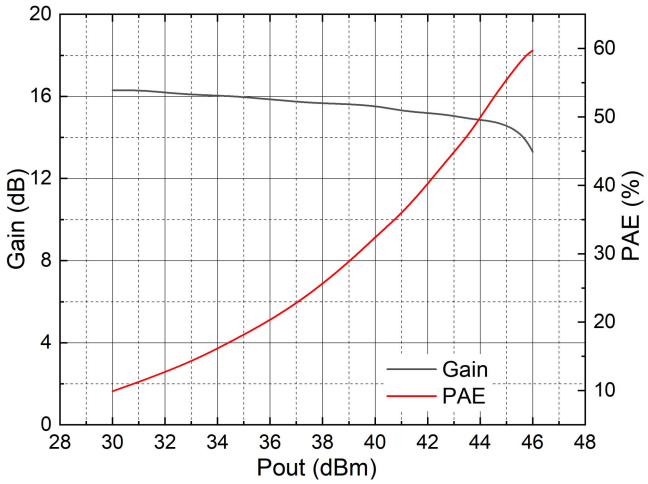
Typical Performance (EVB: 1.9GHz~2.4GHz, Temp=+25°C, V_{DD}=+28V, I_{DQ}=200mA, CW wave test)



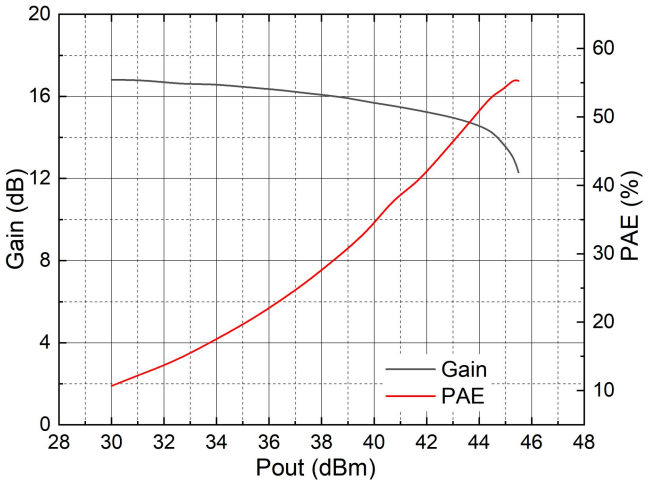
Gain , Input Return Loss vs. Freq



Psat, PEA vs. Freq

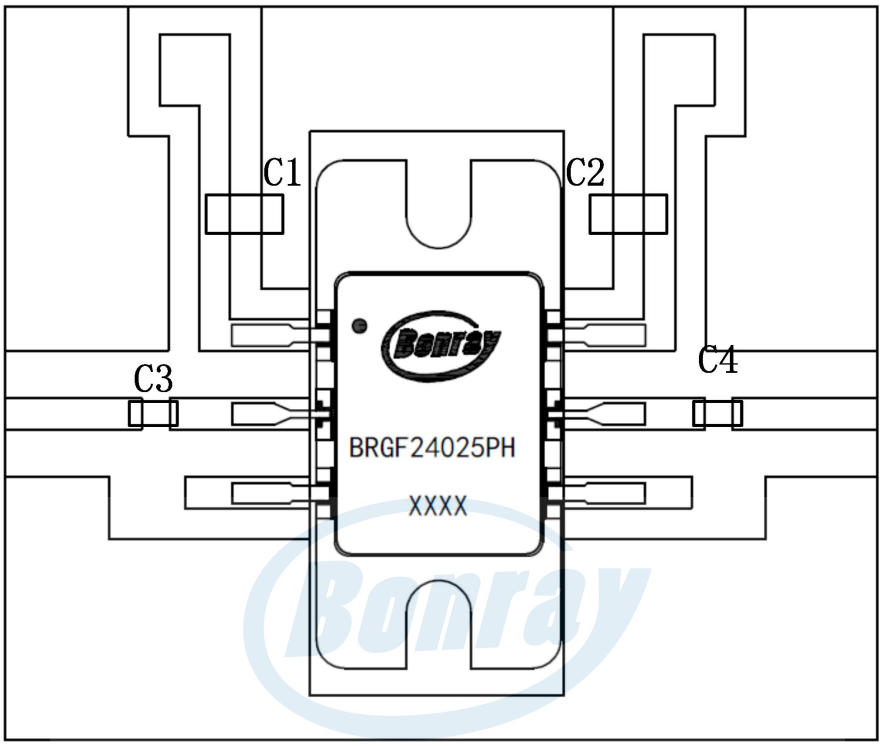


Gain , PEA vs. P_{out} @2GHz

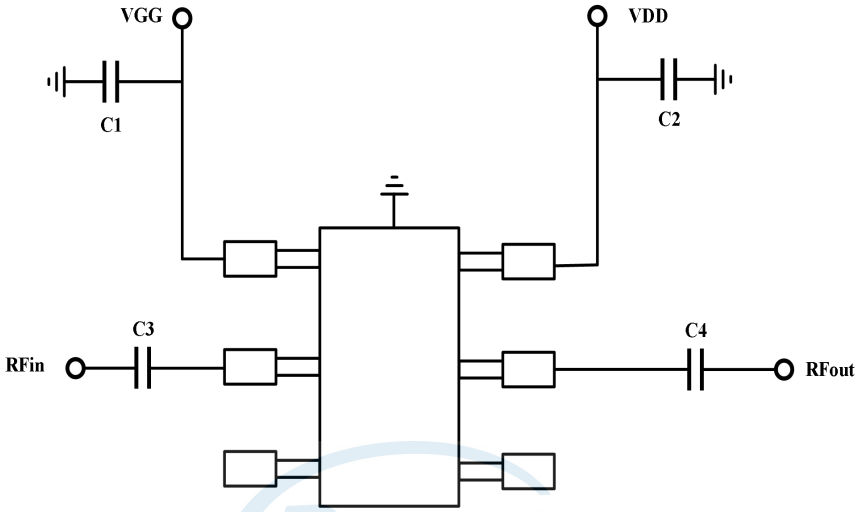


Gain , PEA vs. P_{out} @2.3GHz

PCB Evaluation Board



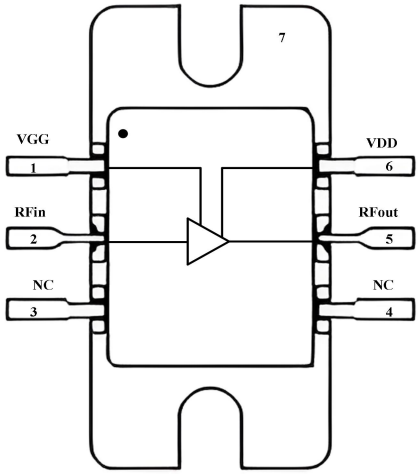
Typical Application Schematic



Bill of Material

Designator	Package	Description	Part Number
U1	Gold Seal	Matched power amplifier in 25W power class	BRGF024025PHG
C4	0805 Patch capacitor	47pF, 250V, 5%	VJ0805D470JXPQJHT
C1,C2	1210 Patch capacitor	10uF, 100V	GRM32EC72A106KE05#
C3	0603 Patch capacitor	2.4pF, 250V	GQM1875C2E2R4BB12#

Pin Configuration and Description



Pin Number	Pin Name	Description
1	VGG	Gate voltage;
2	RFin	RF Input matched to 50 ohms;
3, 4	NC	No connection;
5	RFout	RF Output matched to 50 ohms;
6	VDD	Drain voltage;
7	Metal Housing	Amplifier source level, grounded, cooling

Power-on Sequence

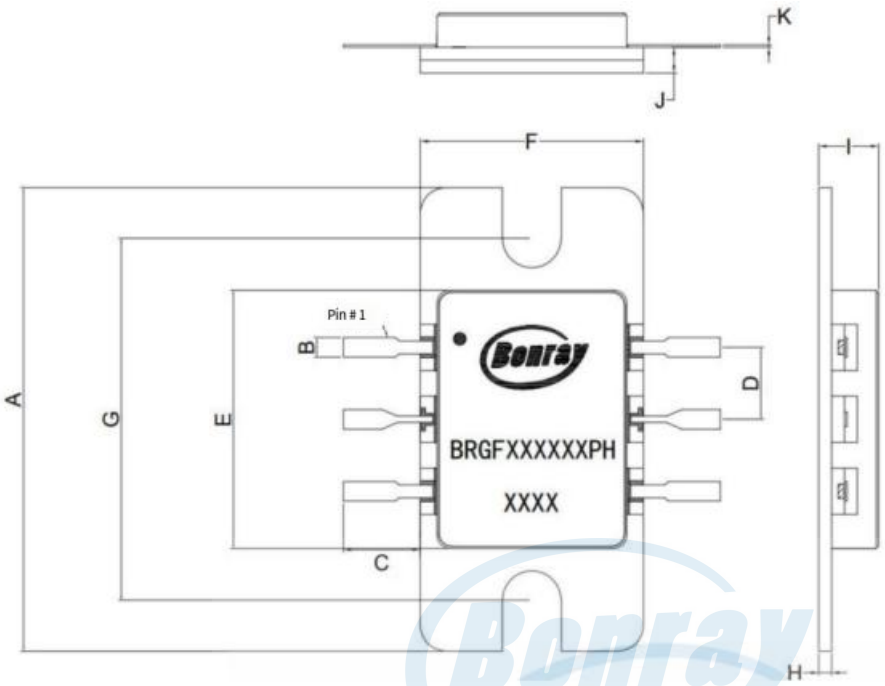
1. Set the grid voltage (V_{GG}) to -5V
2. Set drain voltage (V_{DD}) to +28V, current limit 2.7A
3. Turn on the gate voltage
4. Turn on drain voltage
5. Increase the gate voltage (V_{GG}) so that the drain current is 200mA
6. Input RF signal

Power-off Sequence

1. Turn off the RF signal
2. Reduce the gate voltage (V_{GG}) to -5V
3. Turn off the drain Supply Voltage voltage
4. Turn off the grid Supply Voltage voltage

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



DIM	MILMETER(mm)		
	Min	Avg	Max
A	17.83	18.03	18.23
B	0.63	0.76	0.9
C	2.5	3	3.5
D	2.67	2.8	2.93
E	9.9	10.05	10.2
F	8.55	8.7	8.85
G	13.88	14.08	14.28
H	0.37	0.5	0.63
I	2.25	2.4	2.55
J	0.8	1	1.2
K	0.7	0.1	1.7

Recommended Soldering Temperature Profile