Product Features

Frequency : 10MHz ~ 8GHz

0.25dB attenuation step, maximum attenuation 31.75dB

Insertion Loss: -1.2dB@800MHz

Input Power for 1dB Compression: +36.3dBm@800MHz

Supply Current: 3mA @ Vdd=+5V

Package: QFN24 (4mm×4mm)

Application

Communication Base Stations

Test and Measurement Equipment

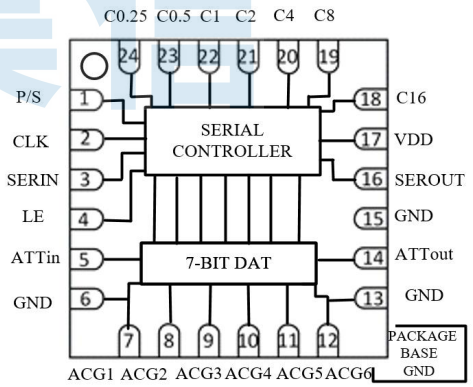
Electronic Countermeasures, Remote Sensing and Telemetry

Short-wave and Ultra-short-wave Wireless Communication Equipment

General Description

The BR9361FPJ is a 7-bit high-precision serial/parallel digital step attenuator fabricated on GaAs process technology, featuring active-high control logic. The operating frequency range is 10MHz ~ 8GHz, the static current is 3 mA when the standard 5V power supply, and the insertion loss is less than 3dB at 10M~8000MHz; The attenuation bits are 0.25, 0.5, 1, 2, 4, 8, 16, the minimum attenuation is 0.25dB, the maximum attenuation is 31.75dB, 7-bit TTL/CMOS control signal is used to control the attenuation state, support three-wire serial input or 7-bit parallel input, to provide users with optional power status and serial output port.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BR9361FPJ	QFN24	10MHz to 8GHz GsAs Digital Attenuator

Electrical Specifications

Parameters		Min.	Typ.	Max.	Units
Insertion Loss	0.01GHz to 8.0GHz	-2.8	-1.2	-1.1	dB
Attenuation Range	0.01GHz to 8.0GHz	0.25	-	31.75	dB
Input Return Loss	0.01GHz to 8.0GHz	-	-20	-	dB
Output Return Loss	0.01GHz to 8.0GHz	-	-19	-	dB
Attenuation Accuracy: (reference insertion loss) All attenuation states	0.01GHz to 1.0GHz 1.0GHz to 4.0GHz 4.0GHz to 8.0GHz	+ / - 0.9 + / - 0.8 + / - 1.0			dB
Output Power for 1dB Compression	0.01GHz to 6GHz	20.5	36.6	37.5	dBm
Input Third-Order Interception	1GHz to 6GHz	42.6	44.5	46.4	dBm
Switching Time T_{rise} (50% CTL-90% RF) T_{fall} (50% CTL-10% RF)	200MHz Attenuation 16dB test	- -	105 68	- -	ns ns
Test Conditions: Vdd=+5V, I=3mA, IIP3 spacing=1MHz, Pin=10dBm/tone, Temp=+25℃					

Absolute Maximum Ratings

Maximum Operating Voltage (Vdd) : +7V

Max RF input Power: +30dBm@100MHz

Control Voltage Range: 0V ~ Vdd

Recommended Working Conditions

Supply Voltage: +5V

Supply Current: 3mA

Control Voltage Threshold: 0 ~ 0.8V (low)

2.7V ~ Vdd (high)

Storage Temperature: -65℃ ~ +150℃

Operating Temperature: -55℃ ~ +125℃

Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and. exposure to absolute-maximum-ratings conditions for extended periods will affect the reliability.

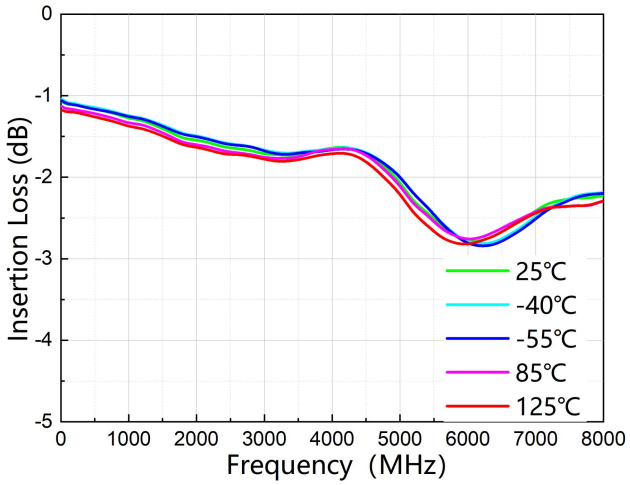
ESD Warnings

ELECTROSTATIC SENSITIVE DEVICE

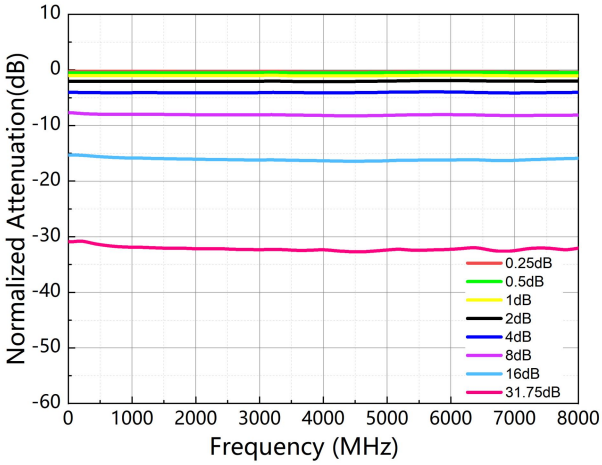
OBSERVE HANDLING PRECAUTIONS

Typical Performance (+5V power supply, parallel control, EVB test results)

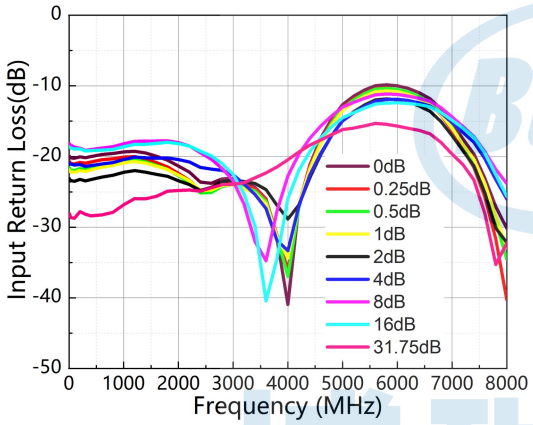
Parameters	Typ.							Units
Frequency	10	50	100	300	800	1000	1400	MHz
Reference State Insertion Loss	-1.1	-1.1	-1.1	-1.1	-1.2	-1.3	-1.4	dB
Attenuation Accuracy (0.25dB)	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	dB
Attenuation Accuracy (0.5dB)	-0.01	-0.01	-0.01	-0.01	-0.01	-0.01	0.01	dB
Attenuation Accuracy (1 dB)	-0.02	-0.02	-0.02	-0.02	-0.03	-0.03	-0.02	dB
Attenuation Accuracy (2 dB)	-0.04	-0.04	-0.04	-0.05	-0.07	-0.07	-0.06	dB
Attenuation Accuracy (4 dB)	-0.02	-0.03	-0.04	-0.07	-0.11	-0.11	-0.10	dB
Attenuation Accuracy (8 dB)	0.32	0.30	0.26	0.09	0.05	0.05	-0.02	dB
Attenuation Accuracy (16 dB)	0.70	0.68	0.68	0.58	0.21	0.14	0.05	dB
Attenuation Accuracy (31.5dB)	0.89	0.86	0.87	0.79	-0.07	-0.14	-0.29	dB
Input Return Loss	-20.0	-20.2	-20.2	-20.2	-19.6	-19.3	-19.5	dB
Output Rrturn Loss	-20.0	-20.2	-20.1	-19.8	-18.8	-18.7	-18.6	dB
Input Power for 1dB Compression	20.5	24.2	26.2	34.9	36.3	36.5	36.9	dBm
Frequency	1800	2000	2600	3000	3600	4000	4500	MHz
Reference State Insertion Loss	-1.5	-1.5	-1.6	-1.7	-1.7	-1.6	-1.8	dB
Attenuation Accuracy (0.25dB)	-0.03	-0.03	-0.04	-0.04	-0.06	-0.08	-0.08	dB
Attenuation Accuracy (0.5dB)	0.01	0.01	0.01	0.01	0.01	-0.01	0.01	dB
Attenuation Accuracy (1 dB)	-0.02	-0.02	-0.02	-0.03	-0.04	-0.06	-0.06	dB
Attenuation Accuracy (2 dB)	-0.06	-0.06	-0.06	-0.06	-0.07	-0.09	-0.07	dB
Attenuation Accuracy (4 dB)	-0.10	-0.11	-0.11	-0.10	-0.10	-0.11	-0.09	dB
Attenuation Accuracy (8 dB)	-0.03	-0.05	-0.08	-0.09	-0.12	-0.20	-0.24	dB
Attenuation Accuracy (16 dB)	-0.02	-0.07	-0.15	-0.20	-0.26	-0.33	-0.42	dB
Attenuation Accuracy (31.5dB)	-0.31	-0.42	-0.55	-0.61	-0.76	-0.54	-1.00	dB
Input Return Loss	-20.5	-21.3	-23.8	-23.1	-26.0	-40.9	-17.4	dB
Output Return Loss	-19.4	-20.4	-21.7	-21.9	-24.4	-39.2	-18.3	dB
Input Power for 1dB Compression	37.1	37.3	37.4	37.1	36.9	36.7	36.4	dBm
Frequency	5000	5500	6000	6500	7000	7500	8000	MHz
Reference State Insertion Loss	-2.1	-2.6	-2.8	-2.6	-2.4	-2.3	-2.2	dB
Attenuation Accuracy (0.25dB)	-0.07	-0.04	-0.04	-0.05	-0.08	-0.11	-0.13	dB
Attenuation Accuracy (0.5dB)	0.02	0.06	0.07	0.05	0.04	0.04	0.04	dB
Attenuation Accuracy (1 dB)	-0.03	0.02	0.03	-0.01	-0.03	-0.04	-0.05	dB
Attenuation Accuracy (2 dB)	0.00	0.08	0.09	0.02	-0.02	-0.02	-0.01	dB
Attenuation Accuracy (4 dB)	-0.02	0.05	0.03	-0.10	-0.14	-0.08	-0.04	dB
Attenuation Accuracy (8 dB)	-0.19	-0.05	-0.04	-0.16	-0.20	-0.12	-0.13	dB
Attenuation Accuracy (16 dB)	-0.35	-0.22	-0.18	-0.27	-0.28	-0.01	0.10	dB
Attenuation Accuracy (31.5dB)	-0.65	-0.66	-0.53	-0.68	-0.81	-0.35	-0.31	dB
Input Return Loss	-12.7	-10.0	-10.0	-11.8	-15.3	-23.1	-30.2	dB
Output Return Loss	-13.3	-10.3	-10.1	-12.3	-15.4	-20.4	-21.9	dB
Input Power for 1dB Compression	36.4	36.8	36.7	-	-	-	-	dBm
Switching Time	105ns (rise switch)				68ns (down switch)			ns
Test Conditions: Vdd=+5V, I=3mA, Temp=+25°C								



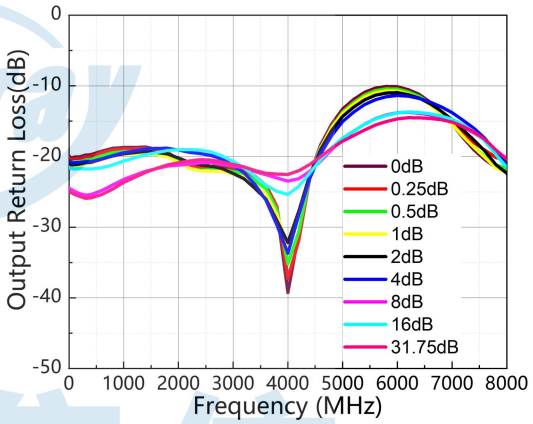
Insertion Loss vs. Frequency



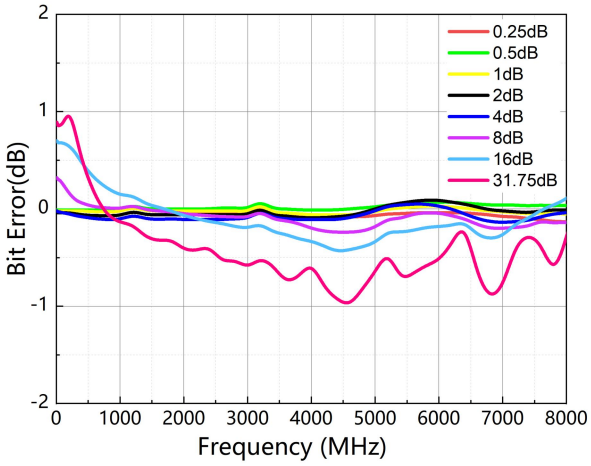
Relative Attenuation vs. Frequency



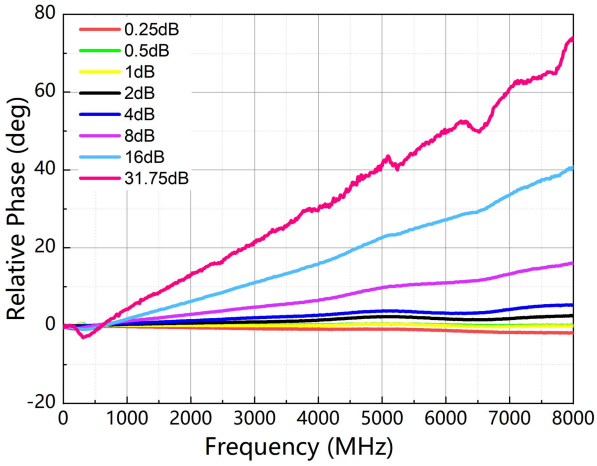
Input Return Loss vs. Frequency



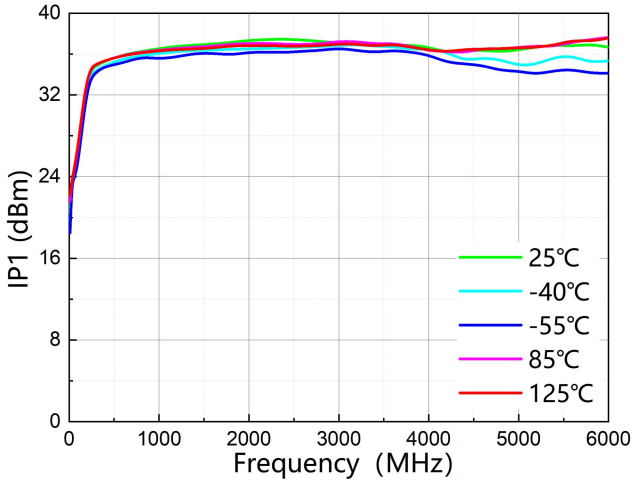
Output Return Loss vs. Frequency



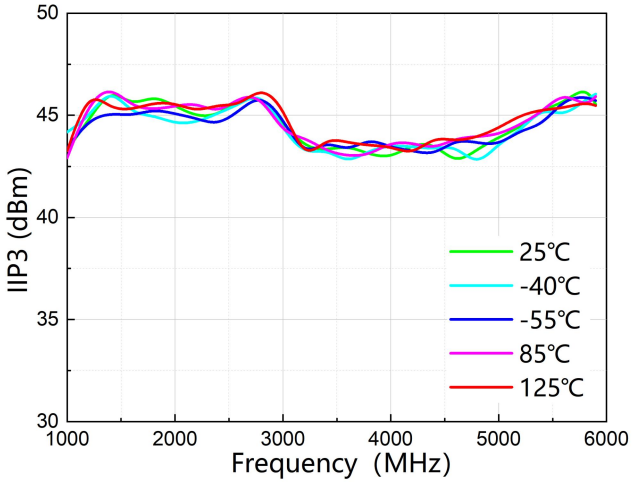
Attenuation Error vs. Frequency



Additional Phase Shift vs. Frequency

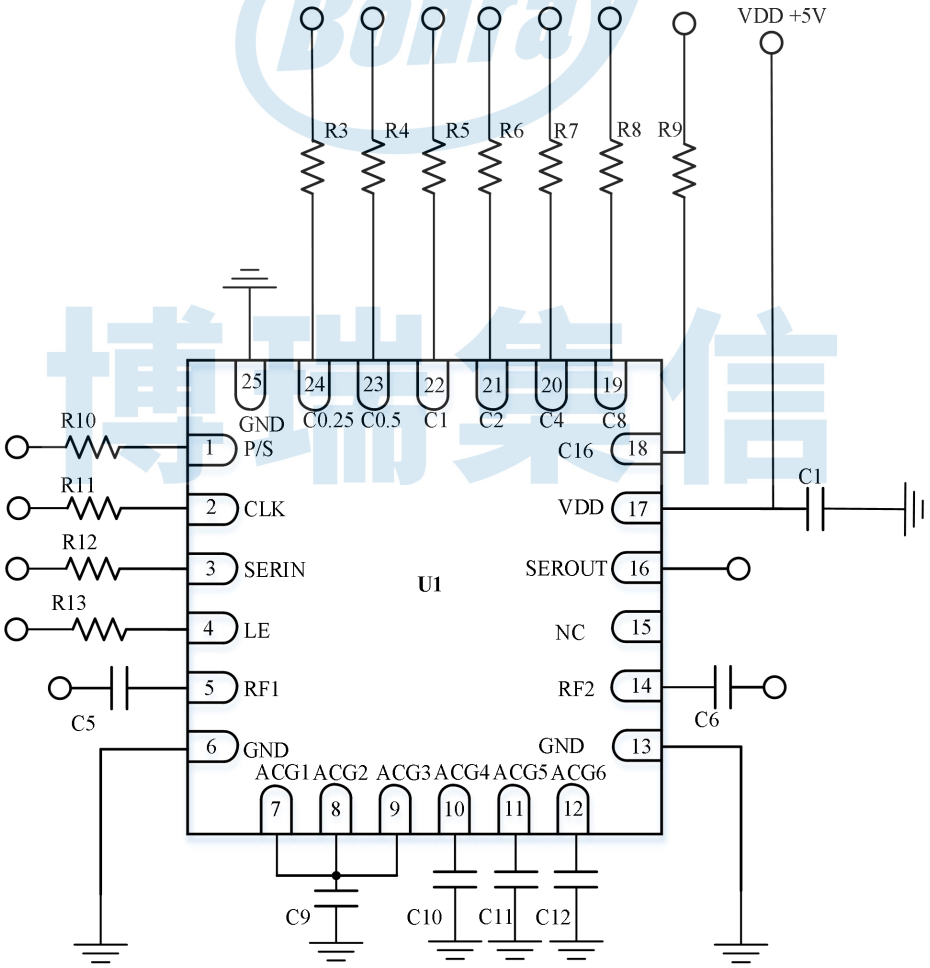


IP1 vs. Frequency



IIP3 vs. Frequency

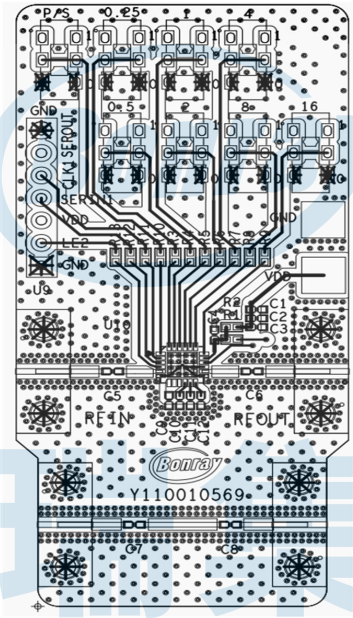
Typical Application Schematic

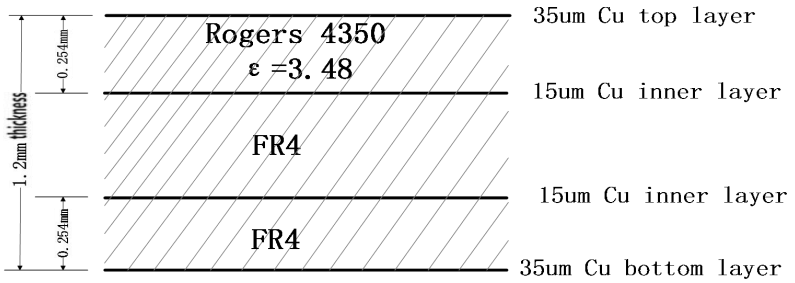


Bill of Material

Component	Package	Value	Part Number
U1	QFN24	High effective attenuator	BR9361FPJ
C1	0402	1nF	GRM1555C1H102JA01D
C5, C6	0402	100nF	GRM155R7H104KE14D
R3~R13	0402	200 Ω	RC0402JR-07200RL
C9,C10,C11,C12	0402	1 u F	GRM155Z71A105KE01D

PCB Evaluation Board

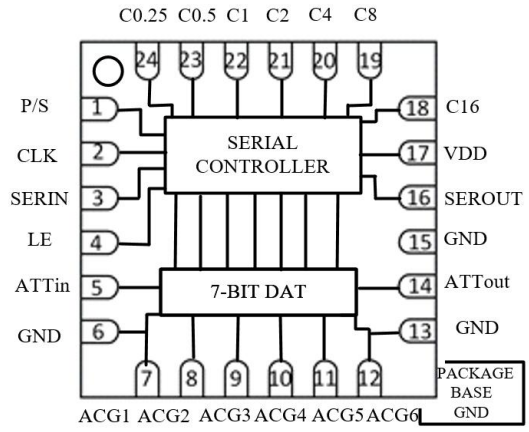




50 ohms Impedance Signal Lines： width=0.53mm, spacing=0.53mm

Note: R1, R2, C3, C4 are reserved bits.

Pin Configuration and Description



Pin Number	Pin Name	Description
1	P/S	String/parallel control pins.
2	CLK	Serial control clock pins.
3	SERIN	Serin 3 Enter data pins in serial.
4	LE	String exercise energy pins.
5, 14	RF1, RF2	The pin is DC coupled and matched to 50 ohms, requiring an additional isolation capacitor, and the capacity Value is determined by the lowest operating frequency.
7 ~ 12	ACG1 ~ ACG6	The external capacitor needs to be connected to the ground, the Value of the capacity is determined by the lowest operating frequency, and the capacitor is placed as close as possible to the pin.
13, 15	GND	Ground pins; This pin and the package substrate must be connected to the RF/DC ground.
16	SEROUT	Output from this pin after 7 clock cycles of serial input data lag.
17	Vdd	Power supply voltage supply pin.
18 to 24	C0.25 ~ C16	Parallel control port. See the control true Value table for the control logic. When parallel control mode is not used, the 7-bit parallel port must be connected to a high or low level and cannot be suspended.
-	EP	Grounded.

Chip Status Selection

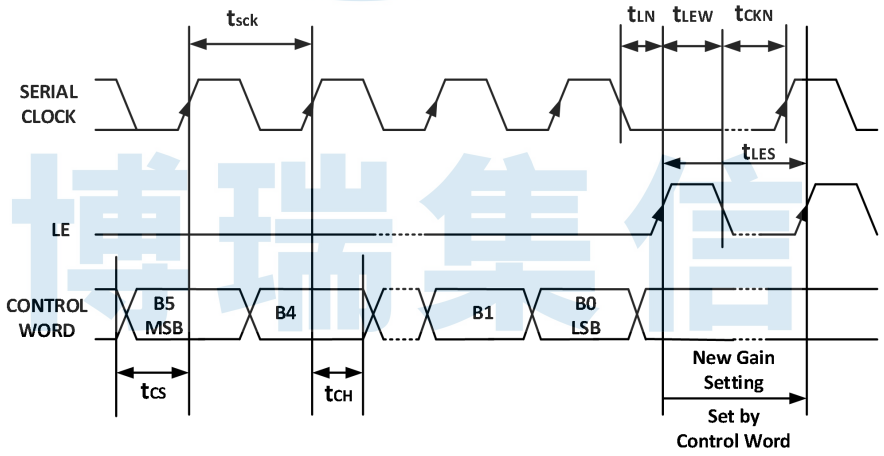
BR9361FPJ has two control methods, namely: serial control and parallel control. The control pins and control true Value for the two states are shown in the following table:

Chip State Selection Control True Value Table

LE	P/S	Chip Status
1	0	Parallel control
1	1	Serial control

Serial Control

The BR9361FPJ is controlled by a 3-wire SPI (SERIN, CLK, LE) digital compatible interface. When P/S=1, the SPI operation is effective, and when it works normally, P/S is high; 7-bit serial data is loaded MSB first; Rising edge trigger clock CLK and LE need to clear conversion; 7 bits of serial data are successively fed into the register and output to the attenuator. At the same time, the CLK is masked to prevent the output state from changing; When LE=0, the output remains unchanged.



Timing Feature Sheet

Number	Parameters	Typ.	Number	Parameters	Typ.
1	Minimum clock period (tSCK)	100ns	5	Minimum LE pulse duration (tLEW)	10ns
2	Control signal setup time (tCS)	20ns	6	Minimum LE pulse interval time (tLES)	630ns
3	Control signal hold time (tCH)	20ns	7	Serial clock hold time (tCKN) from LE	10ns
4	LE signal setup time (tLN)	10ns			

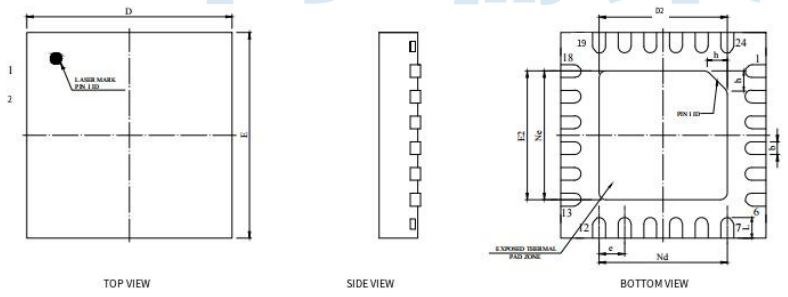
Parallel Control

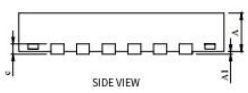
When parallel control is adopted, LE=1, P/S=0, the control true Value table is as follows:

Parallel Control Voltage True Value Table

Control Voltage Input							Attenuated State RF1/RF2
C16 16dB	C8 8dB	C4 4dB	C2 2dB	C1 1dB	C0.5 0.5 dB	C0.25 0.25 dB	
0	0	0	0	0	0	0	Reference state insertion loss
0	0	0	0	0	0	1	0.25 dB
0	0	0	0	0	1	0	0.5 dB
0	0	0	0	1	0	0	1 dB
0	0	0	1	0	0	0	2 dB
0	0	1	0	0	0	0	4 dB
0	1	0	0	0	0	0	8 dB
1	0	0	0	0	0	0	16 dB
1	1	1	1	1	1	1	31.75 dB
Note: Any combination of the above decay states will provide an amount of decay approximately equal to the sum of the attenuation of the selected bits.							

Package Dimensions (mm)





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.80	0.85
A1	0.01	0.02	0.05
b	0.20	0.25	0.30
c		0.270REF	
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
L	0.35	0.40	0.45
h	0.35	0.40	0.45