Product Features

RMS Response

Excellent Temperature Stability

Maximum input Power of 22 dBm

Linear Response Frequency up to 1.8GHz

Single-Power Supply Voltage: 2.7V to 5.5V

Low Power Consumption: 11.4mW on 3V Supply Voltage

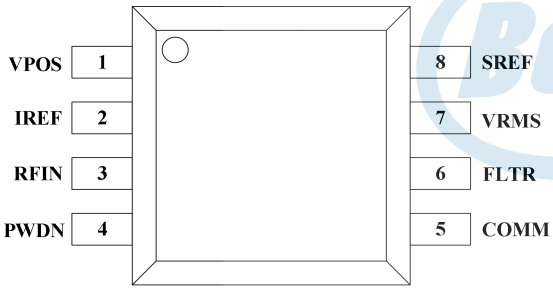
Off Mode, current less than 1mA

General Description

The BR9262EAJ is an RMS power detector with RF signal input frequency up to 1.8GHz. This chip is simple and easy to use, only requires a single power Supply Voltage, the power supply voltage is between 2.7V and 5.5V, and the other needs a power decoupling capacitor and an input signal coupling capacitor, which can meet most applications. The output of the BR9262EAJ is a linear response to the input signal with a typical gain of 6.5V/V rms.

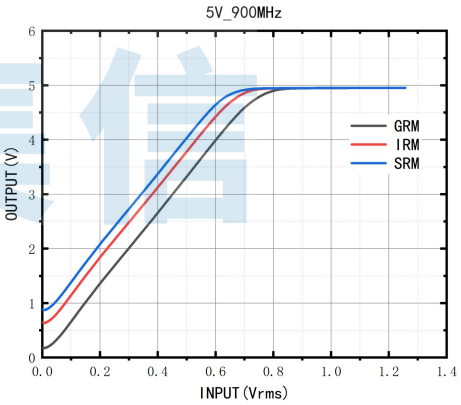
The BR9262EAJ can be used to detect simple and complex waveforms, and is particularly suitable for detecting peak-to-average ratio signals such as CDMA and W-CDMA signals.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BR9262EAJ	eMSOP8	2 MHZ to 1.8 GHz Power Detector



Output in Three Modes, 5V, 900MHz

The BR9262EAJ has three operating modes to suit the needs of different analog-to-digital converters:

1. Ground reference mode (GRM), the mode reference voltage is 176mV;

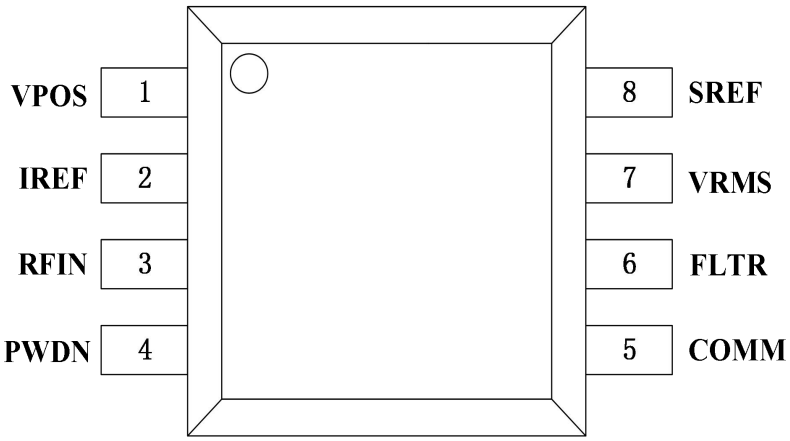
2. Internal reference mode (IRM), the reference voltage of this mode is 663mV;

3. Power reference mode (SRM), the mode reference voltage is 874mV.

Electrical Specifications (TA=25 ° C, unless otherwise stated, Vs=3V, f_{RF}=100MHz, GRM mode)

Parameters	Conditions	Min.	Typ.	Max.	Units
Frequency Range	Rf input	-	-	1.8	GHz
Linear input Maximum	Vs=3V	-	452	-	mV (RMS)
	Vs=5V	-	760	-	
Input impedance		-	11.2 M	-	Ω
Ac-dc Conversion Gain					
RMS Conversion Gain	f=100MHz Vs=5V	4.0	-	10.5	V/Vrms
Dynamic Range CW Input, −55°C < TA < +125°C	Effective Dynamic Range	25	-	28	dB
Reference Pattern					
GRM Reference Mode Output Voltage Reference	SREF=0, IREF=Vs, f=100MHz, Vs=5V	90	-	270	mV
Output Voltage Reference in IRM Reference Mode	SREF=0, IREF open circuit, f=100MHz, Vs=5V	520	-	1040	mV
Output Voltage Reference in SRM Reference Mode	SREF=3V, IREF=3V, f=100MHz, Vs=3V	370	-	800	mV
	SREF=5V, IREF=5V, f=100MHz, Vs=5V	630	-	1200	mV
Power Down Mode					
PWDN High level Threshold	2.7 ≤ Vs ≤ 5.5 V	V - 0.5 -	-	-	V
PWDN Low level Threshold	2.7 ≤ Vs ≤ 5.5 V	-	-	0.1	V
Power-up Response Time	10 pF at FLTR,Vs=5V Pin=0dBm at RFIN	-	386	-	ns
	100 pF at FLTR ,Vs=5V Pin=0 dBm at RFIN	-	541	-	ns
PWDN Bias Current at High level	Vs=3V	-	3	-	Mu A
	Vs=5V	-	300	1000	Mu A
Power Supply					
Range	- 55 ℃ ~ + 125 ℃	2.7	-	5.5	V
Quasi-static Current	RFIN=0 PWDN Low level	-	3.8	-	mA
Turn off Status Current	RFIN=0, PWDN high	-	3	1000	Mu A

in Configuration and Description



Pin Number	Pin Name	Description
1	VPOS	Power supply voltage, 2.7~5.5V.
2	IREF	Output reference control. When the Reference Designator operates in IRM mode, the pin is open. In other modes, the pin should be connected to VPOS and not grounded.
3	RFIN	Signal input, which must be coupled via AC.
4	PWDN	Low power control. When the Reference Designator is operating in detection mode, the logic level is low (below 100mV). When the logic level is high (above Vs-0.5V), the Reference Designator will be turned off and the current will be approximately zero (GRM and IRM mode current below 1000μA, SRM mode current is the supply voltage divided by 100 kω).
5	COMM	Ground pin.
6	FLTR	By connecting a capacitor between this pin and the VPOS, the bandwidth of the internal filter can be made lower.
7	VRMS	Output pins. Close to rail-to-rail output with limited output drive capability. Output load recommended >10kΩ to ground impedance.
8	SREF	Power reference mode control. When using SRM mode, you need to connect to VPOS; Otherwise, it should be connected to COMM(ground).

Absolute Maximum Ratings

Power Supply Voltage: 6V

SREF, PWDN: 0V, Vs

IREF: VS-0.3V, Vs

RFIN: 2.8V rms (50Ω is equivalent to 22dBm)

Recommended Operating Conditions

Power Supply Voltage: 2.7~5.5V

Operating Current: 3.8mA(3V power supply)

Operating Temperature: -55℃~+125℃

Storage Temperature Range: -60℃~+150℃

ESD Class: Class 3B

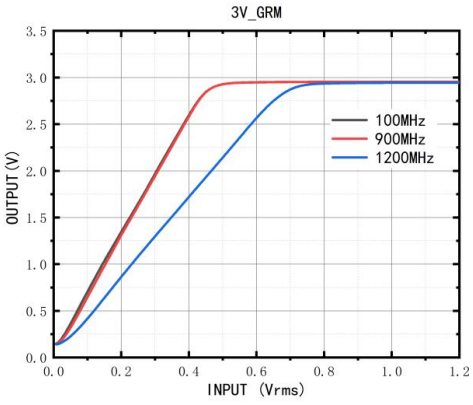
Note: If the above limits are exceeded during Application, permanent damage may be caused to the chip, and the working performance of the chip cannot be guaranteed. If the long-term Application under the maximum limit conditions, the reliability of the chip can not be guaranteed.

ESD WARNING

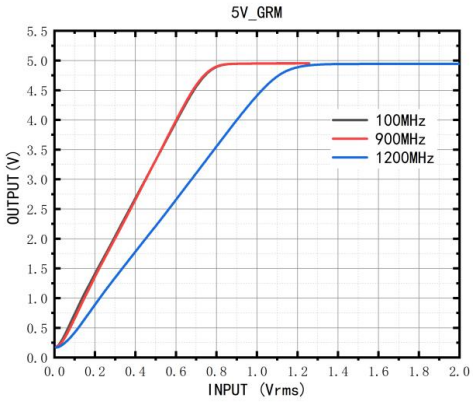
ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

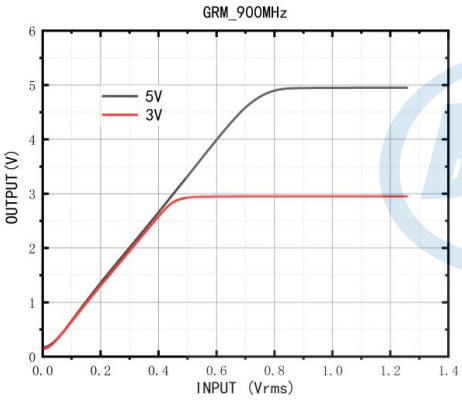
Typical Performance



GRM mode, input/output curves at 3V

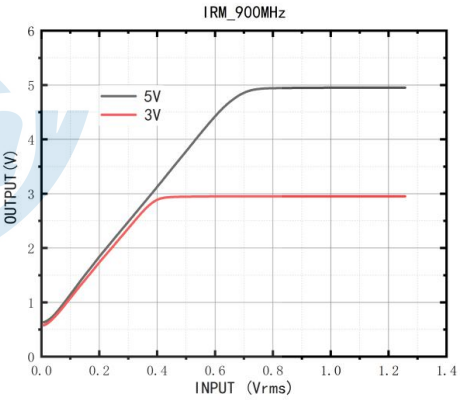


GRM mode, input/output curves at 5V



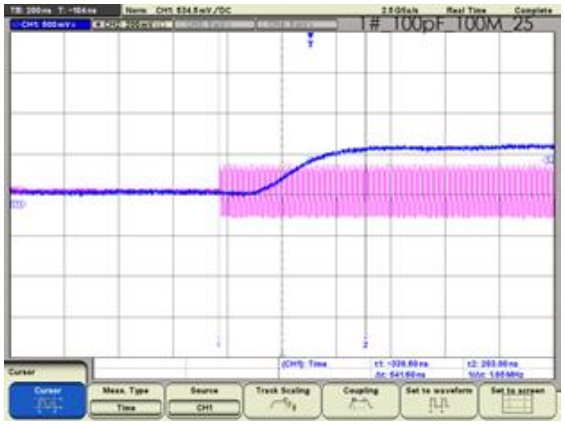
900MHz,5V

Input/Output curve in GRM mode



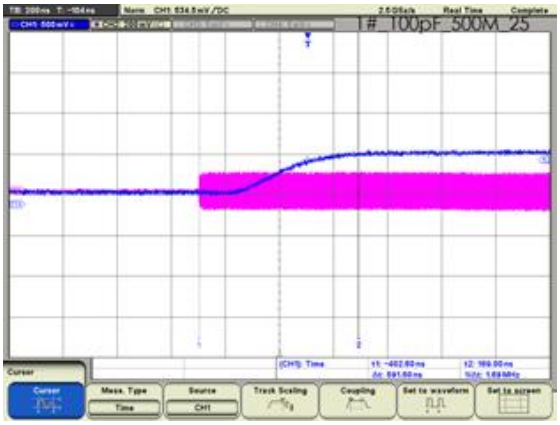
900MHz,5V

Input/Output curve in IRM mode



100MHz, C_{FLTR}=100pF

Response time in GRM mode



500MHz, C_{FLTR}=100pF

Response time in GRM mode

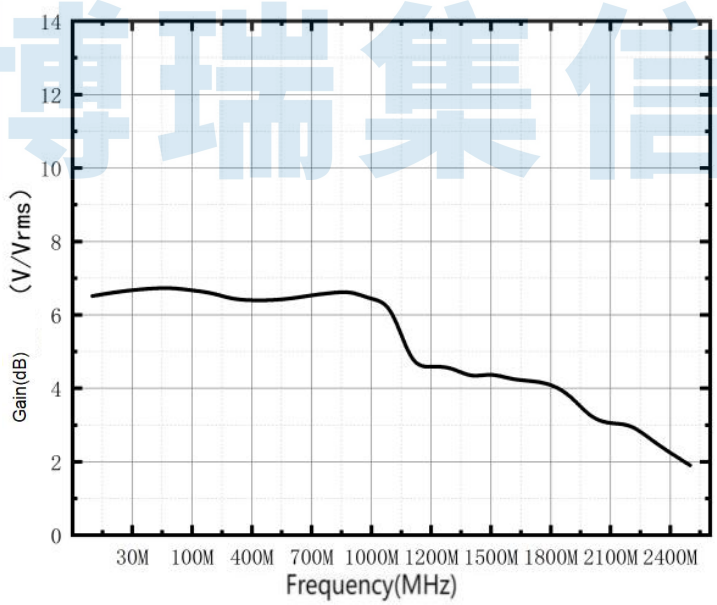
Circuit Principle

The BR9262EAJ uses a high-precision error amplifier to balance the output of two identical square units, thus realizing the power detection function of this product.

The BR9262EAJ responds to the voltage of the input signal V_{IN} to produce a current squared to that voltage, which flows through the load to produce a voltage. The output terminal is connected to the capacitor, forming a low-pass filter, and the output of the filter is the square mean of the input V_{IN}. The filter output voltage is connected to the error amplifier, at the same time, the exact same square circuit as a negative feedback, connected to the output and input of the error amplifier, due to the high gain of the operation amplifier, the output of the two square circuits is equal, so the input of the square circuit on the feedback path (that is, the error amplifier output) is equal to the root-mean-square voltage of the input signal. The error amplifier output is connected to a fixed Power Gain amplifier with a Power Gain of 6.5@900MHz, i.e. :

$$V_{OUT} = 6.5 \times V_{IN}rms$$

The curve of Power Gain changing with the input frequency is shown in the figure below:



Typical Application

Figure 11~ Figure 13 is the basic circuit connection scheme of BR9262EAJ (EMSOP8 package) three working modes. In each mode, the BR9262EAJ only needs a single power supply, and the voltage range is 2.7~5.5V. Two decoupling capacitors of 100pF and 0.01μF need to be connected to the VPOS pin. When the PWDN pin is connected to VPOS, the Supply Current can be reduced from 3.8mA in normal working condition to less than 1mA.

The input should be connected to an external bypass resistor and coupling capacitor to achieve broad band approximate 50Ω impedance matching. The relationship between the input impedance and the coupling network is discussed in detail below.

The input coupling capacitance and the input resistance inside the chip together determine the corner frequency of the input

$$f_{-3dB} = \frac{1}{2\pi C_8 R_{IN}}$$

If the 100pF capacitor shown in Figures 11 to 13 is used, the corner frequency is around 10kHz.

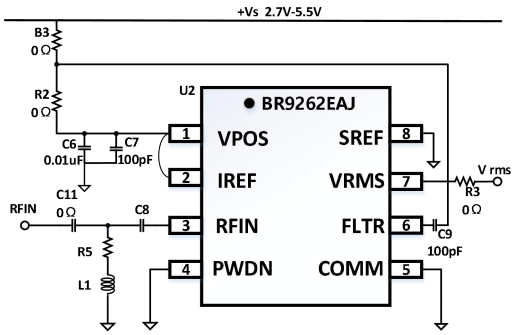


Figure 11 Block Diagram of Basic Connecting Circuit in GRM Mode

The output voltage is 6.5 times that of the input signal Vrms (conversion Power Gain is 6.5V/V rms). Different operating modes can be adjusted by setting SREF and IREF. The mode shown in Figure 11, under the condition of 5V supply voltage, the output swing is 0~4.9V, and the other two modes will add different offset voltages to the output voltage.

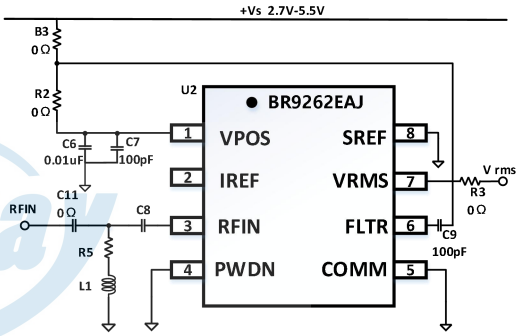


FIG. 12 Basic circuit Diagram of IRM Mode

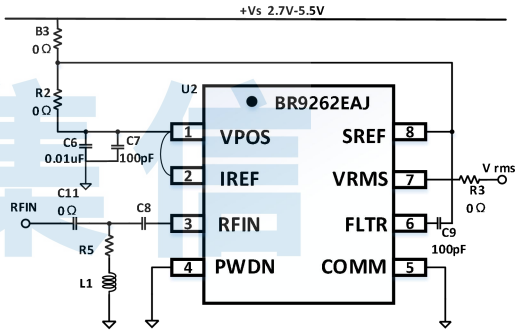


Figure 13 Basic Connection Circuit Block Diagram of SRM Mode

In the internal reference mode (Figure 12), the output voltage will increase the offset by 350mV. In power reference mode (Figure 13), the output voltage will increase the offset of Vs/6.5. Table 4-1 and Table 4-2 describe the connection mode, output swing, and minimum output voltage for each operating mode in the high and low frequency

bands.

Table 4-1 Operating Mode Characteristics (Low frequency)

Modes	IREF	SREF	Output (V)
GRM	VPOS	COMM	$6.5V_{IN}$
IRM	OPEN	COMM	$6.5 + 0.V_{IN}35$
SRM	VPOS	VPOS	$6.5 + V_{IN}$ $6.5V_S/$

Table 4-2 Operating Mode Characteristics (high frequency)

Modes	IREF	SREF	Output (V)
GRM	VPOS	COMM	$4V_{IN}$
IRM	OPEN	COMM	$4V_{IN}+0.35$
SRM	VPOS	VPOS	$4V_{IN}+V_S/4$

Output Swing

FIG. 14 shows the output voltage curves of BR9262EAJ in three operating modes under 5V operating conditions. As can be seen in the figure, both the internal reference mode and the power reference mode reduce the effective dynamic range of the Reference Designator. Lowering the voltage range causes the same problem.

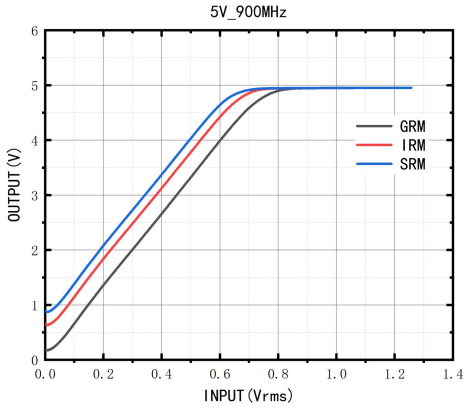


Figure 14 Output Swing for Three Operating Modes

Dynamic Range

The BR9262EAJ is a linear gain system with a typical gain of 6.5V/Vrms, and the dB value of its dynamic range cannot be visually displayed in Figure 15. While the input power dB increases in steady steps, the output power grows at a rate (with dB) that increases in steps. Figure 15 illustrates the relationship between the output growth rate (V/Vrms) and the input Vrms growth rate.

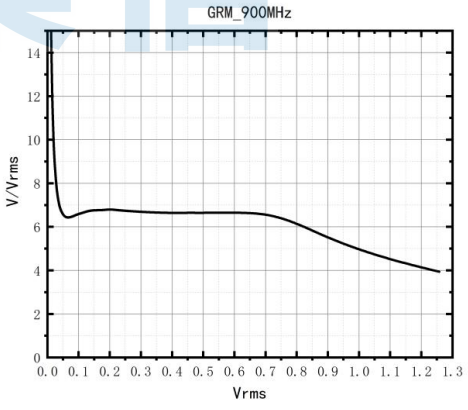


Figure 15 Relation of Gain to input Voltage

Output Coupling and Matching

Input impedance matching adopts high frequency and low frequency segmented matching. For full frequency Application, as shown in Figure 16, the gain of low and high frequency bands is adjusted by using the frequency response of inductor L1, so that the gain of low band converges to 6.5V/Vrms and the gain of high band converges to 4.2V/Vrms. For a single frequency, resonance matching can be used. The optimum value of the matching resistance can be found on the Smith original drawing.

Table 5 shows a list of recommended matching resistance and inductance values for low and high frequency conditions.

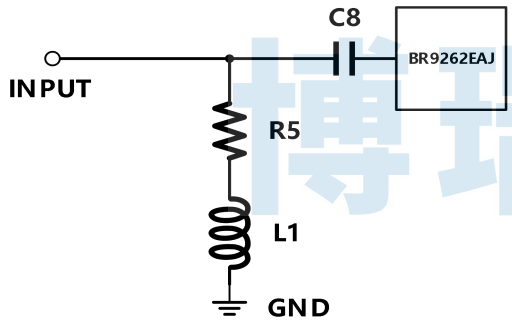


Figure 16 Impedance Matching Network

Table 5 Impedance Matching Relationship

Frequency	L1/nH	R5 / Ω	C8
2 MHZ to 1.1 GHz	5.1	36	2nF
1.1 GHz to 1.8 GHz	3	33	10pF

Power, Enable, and Power on

The static current of the BR9262EAJ is about 3.8mA, and there is not much difference in static power consumption under different supply voltage and input amplitude conditions.

The BR9262EAJ can be turned off by connecting the PWDN (pin 4) to the VPOS or by turning off the power. After turning off, the chip leakage current is less than 1000μA.

When the BR9262EAJ is in the off state (PWDN=VPOS) input signal, the leakage current will increase, and the increase amplitude is related to the amplitude of the input signal.

Voltage and dBm Conversion

In many charts, the abscissa needs to be converted between Vrms voltage and dBm. In general, dBm is calculated relative to the 50Ω impedance. In a 50Ω system, the conversion between dBm and voltage can be performed using the following formula.

$$\text{Power(dBm)} = 10\lg\left[\frac{(V_{\text{rms}})^2}{\frac{50\Omega}{0.001}}\right]$$

$$= 10\lg[20(V_{\text{rms}})^2]$$

$$V_{\text{rms}} = \sqrt{0.001 \times 50\Omega \times \log^{-1}\left(\frac{\text{P(dBm)}}{10}\right)}$$

$$= \sqrt{\frac{\log^{-1}\left(\frac{\text{P(dBm)}}{10}\right)}{20}}$$

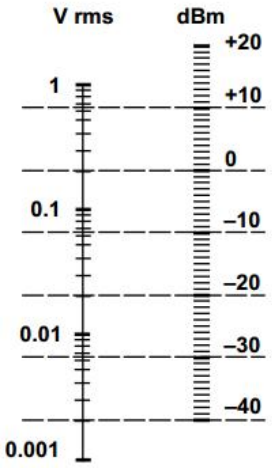


Figure 17 The Conversion between dBm and Vrms Voltage

Output Drive Capability and Output Buffer

The BR9262EAJ can output about 3mA of current. If a larger drive current is required, a simple output buffer circuit can be added.

Typical Application Schematic

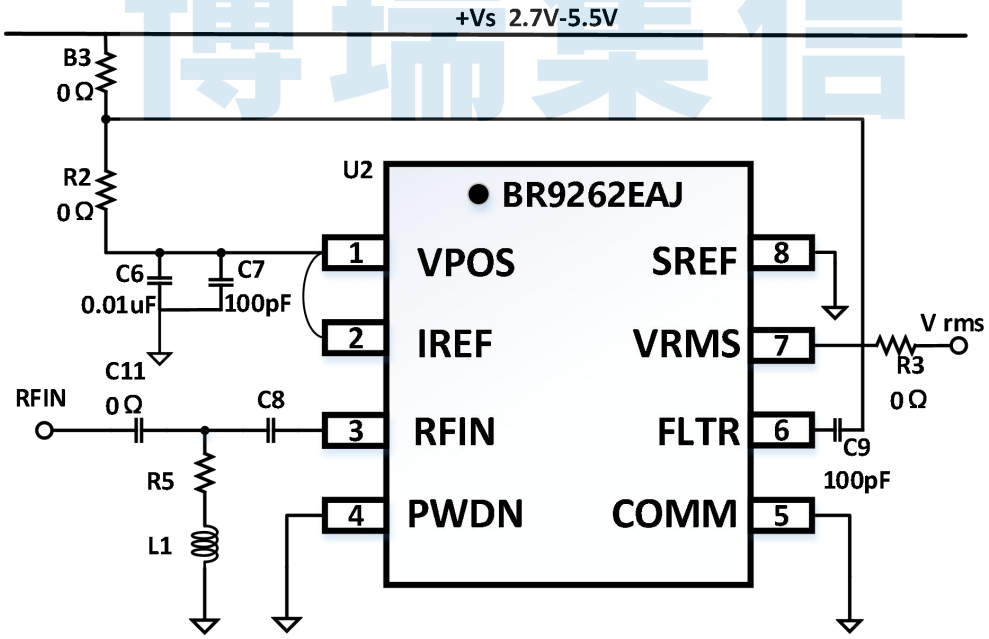


Figure 18

Bill of Material (2MHz~1.1GHz)

Designator	Package	Description	Part Number
C6	0603	0.01 uF	CC0603KRX7R7BB103
C7,C9	0603	100pF	GRM1885C2A101JA01
C8	0603	2nF	C0603C103J4GACAUTO
L1	0402	5.1 nH	LQW15AN5N1B00D
R2, R3, C11	0402	0Ω 0402	RC0402FR-070RL
R5	0402	36Ω 0402	RC0402FR-0736RL
B2,B3[2]	FB0603	220 Ω @ 100 MHZ / 2200 ma	Magnetic Bead, UPZ1608U221-2R2TF

1. The C11 bit number actually uses 0 ohm line for short-circuit processing;

2. B2, B3 bit number is recommended to use magnetic beads, can effectively suppress the interference of the power supply, can also use 0 ohm line short-circuitry instead.

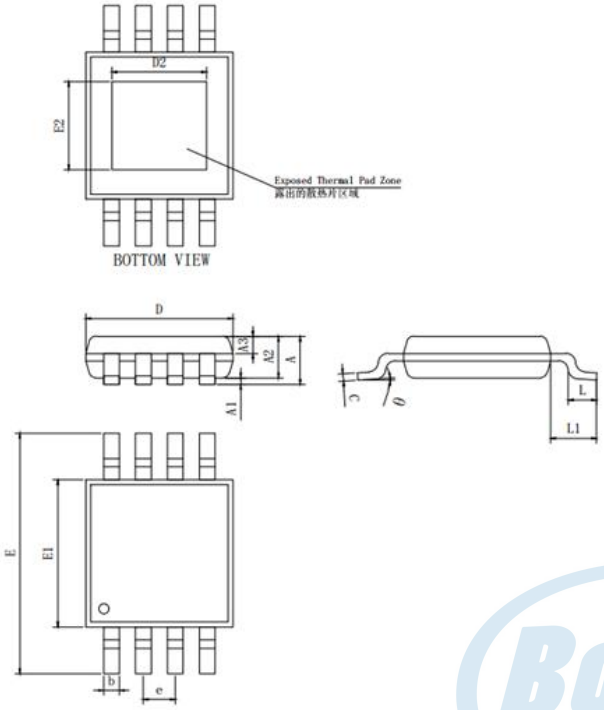
Bill of Material (1.1GHz~1.8G)

Reference Designator	Package Size	Value	P/N
C6	0603	0.01 uF	CC0603KRX7R7BB103
C7, C9	0603	100pF	GRM1885C2A101JA01
C8	0603	10pF	GRM1885C2A100JA01
L1	0402	3nH	LQW15AN3N0B00D
R2, R3, C11	0402	0 Ω	RC0402FR-070RL
R5	0402	33 Ω	RC0402JR-0733RL
B2,B3[2]	0603	220 Ω @ 100 MHZ / 2200 ma	Magnetic Bead, UPZ1608U221-2R2TF

1. C11 bit number actually uses 0 ohm line to do short-circuit processing;

2. B2, B3 bit number is recommended to use magnetic beads, can effectively suppress the interference of the power supply, can also use 0 ohm line short-circuitry instead.

Package Dimensions (mm)



SYMBOLS	Millimeter		
	Min.	Nominal	Max.
A	-	-	1.1
A1	0	-	0.13
A2	0.75	0.85	0.95
A3	0.3	0.35	0.4
b	0.28	-	0.36
c	0.15	-	0.19
D	2.9	3	3.1
E	4.68	-	5.08
E1	2.9	3	3.1
e	0.65 BSC		
L	0.4	-	0.8
L1	0.95 REF		
Theta.	0	-	8 °
D2	1.93 REF		
E2	1.57 REF		

Figure 19