Product Features

RMS Response

Excellent Temperature Stability

560mV rms, 25dBm Maximum Pin (dBm)

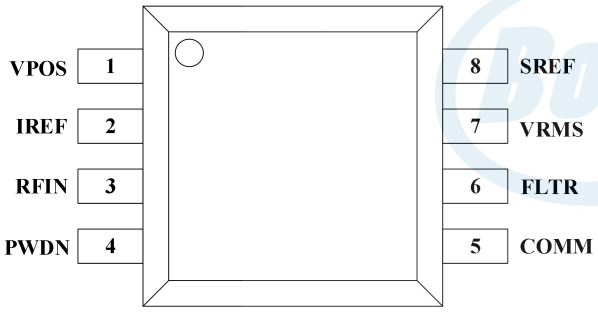
Linear Response Frequency up to 2.5GHz

Single-power Supply Voltage: 2.7V to 5.5V

Low Power Consumption: 1.2mW on 3V Supply Voltage

Off Mode, current less than 1μA

Functional Block Diagram



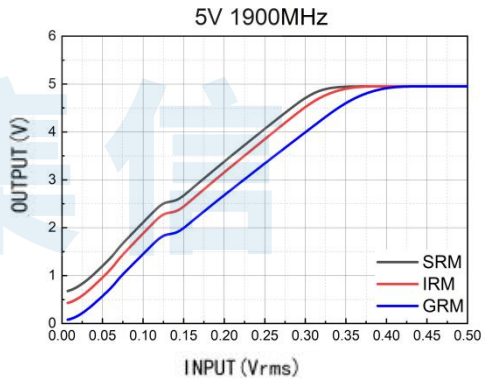
Ordering Information

Part Number	Package	Description
BR9261	MSOP8	2 MHZ to 2.5 GHz Power Detector

General Description

BR9261 is a radio frequency input frequency 2MHz~2.5GHz RMS power detector. This chip is simple and easy to use, only requires a single power Supply Voltage, the power supply voltage is between 2.7V and 5.5V, and the other needs a power decoupling capacitor and an input signal coupling capacitor, which can meet most applications. The output of the BR9261 is a linear response to the input signal with a typical gain of 6.5V/V rms.

The BR9261 can be used to detect both simple and complex waveforms, and is particularly suitable for detecting peaking ratio signals such as CDMA and W-CDMA signals.



Output in Three Modes, 5V, 1900MHz

The BR9261 has three operating modes to suit the needs of different analog-to-digital converters:

1. Ground reference mode (GRM), the mode reference voltage is about 80mV@5V;
2. Internal reference mode (IRM), the reference voltage of which is about 410mV@5V;
3. Power reference mode (SRM), the reference voltage of this mode is about 680MV-@5V.

Electrical Specifications (TA=25 ° C, unless otherwise stated, Vs=3V, f_{RF}=100MHz, GRM mode)

Parameters	Conditions	Min.	Typ.	Max.	Units
Frequency Range	Rf input	-	-	2.5	GHz
Linear input Maximum	Vs=3V	-	-	178	mV (RMS)
	Vs=5V	-	-	316	
Peak-to-average Ratio vs. CW Detection Error	5dB peak-to-average ratio,Vs=5V Modulation type: QPSK Coefficient of roll down: 0.22 Bit rate: 3.84Msps	-	0.07	-	dB
Input Impedance		-	150k	227k	Ω
Ac-dc Conversion Gain					
RMS Conversion Gain (G)	f=100MHz Vs=5V	8	-	18	V/Vrms
Dynamic Range CW Input, −55°C < TA < +125°C	Effective Dynamic Range	-	27	-	dB
Reference Pattern					
GRM Reference Mode Output Voltage Reference	SREF=0, IREF=Vs, Vs=5V	-50	67	150	mV
Output Voltage Reference in IRM Reference Mode	SREF=0, IREF open circuit, Vs=5V	-	415	500	mV
Output Voltage Reference in SRM Reference Mode	SREF=3V, IREF=3V, Vs=3V	-	391	-	mV
	SREF=5V, IREF=5V, Vs=5V	-	664	790	mV

Power Down Mode					
PWDN High level Threshold	2.7 ≤ Vs ≤ 5.5V, −55°C < TA <+125°C	V - 0.8 -	-	-	V
PWDN Low level Threshold	2.7 ≤ Vs ≤ 5.5V, −55°C < TA <+125°C	-	-	V - 1.8 -	V
Power-up Response Time	3 pF at FLTR Pin, 2 dBm at RFIN, Vs=5V	-	18.2	-	Mu s
	100 pF at FLTR Pin, 2 dBm at RFIN, Vs=5V	-	23.5	-	Mu s
PWDN Bias Current at High level	-	-	0.5	1	Mu A
Power supply					
Range	- 55 ℃ ~ + 125 ℃	2.7	-	5.5	V
Quasi-static Current	RFIN=0 PWDN Low level	-	438	-	uA
Turn off Status Current	RFIN=0, PWDN high	-	0.48	1	Mu A

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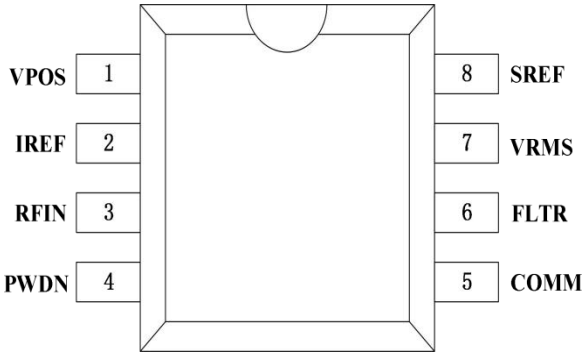
Pin Configuration and Description



Pin Number	Pin Name	Description
1	VPOS	Power supply voltage, 2.7~5.5V.
2	IREF	Output reference control, when the device is operating in IRM mode the pin is open, other mode the pin should be connected to VPOS, not grounded.
3	RFIN	The signal input must be coupled through AC.
4	PWDN	Low power control. When the device is operating in detection mode, connect the logic low level (below Vs~1.8V). When connected to a logic high level (above Vs~0.8V), the device will be turned off and the current will be approximately zero (GRM and IRM mode current below 1μA, SRM mode current is the supply voltage divided by 100kΩ).
5	COMM	Ground pin.
6	FLTR	By connecting a capacitor between this pin and the VPOS, the bandwidth of the internal filter can be made lower.
7	VRMS	Output pins. Close to rail-to-rail output with limited output drive capability. Output load recommended >10kΩ to ground impedance.
8	SREF	Power reference mode control. When using SRM mode, you need to connect to VPOS; Otherwise, it should be connected to COMM(ground).

Absolute Maximum Ratings

Power Supply Voltage: 6V

SREF, PWDN: 0V, Vs

IREF: VS-0.3V, Vs

RFIN: 3.98V rms (50Ω equivalent to 25dBm)

Recommended Operating Conditions

Power Supply Voltage : 5V

Working Current: 0.60mA

Working Temperature: -55℃~+125℃

Storage Temperature range: -60℃~+150℃

ESD Grade: Class 1A

Note: If the above limits are exceeded during Application, permanent damage may be caused to the chip, and the working performance of the chip cannot be guaranteed. If the long-term Application under the maximum limit conditions, the reliability of the chip can not be guaranteed.

ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

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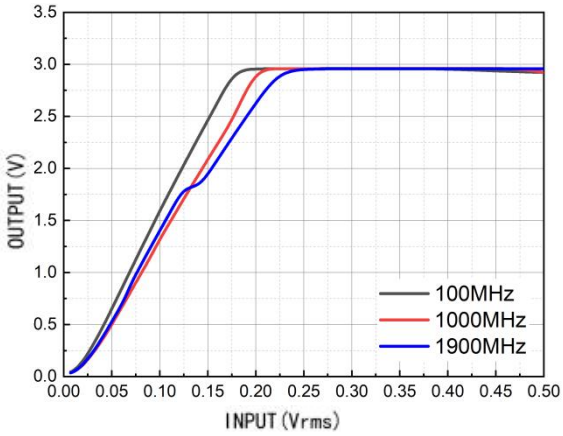
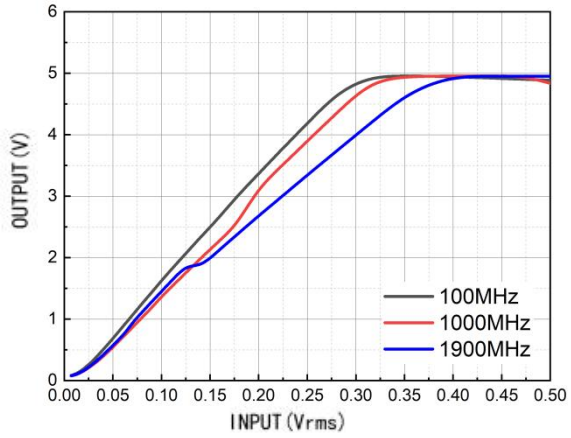
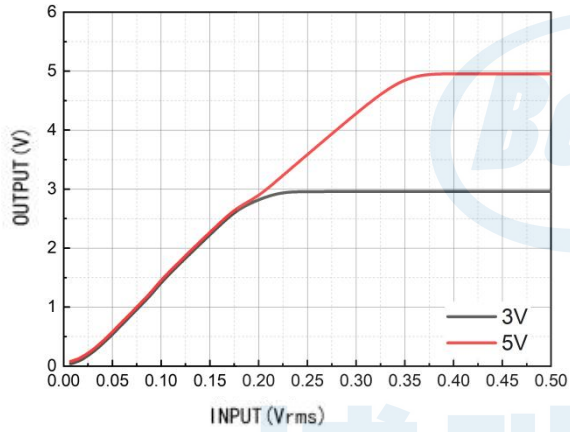
Typical Performance



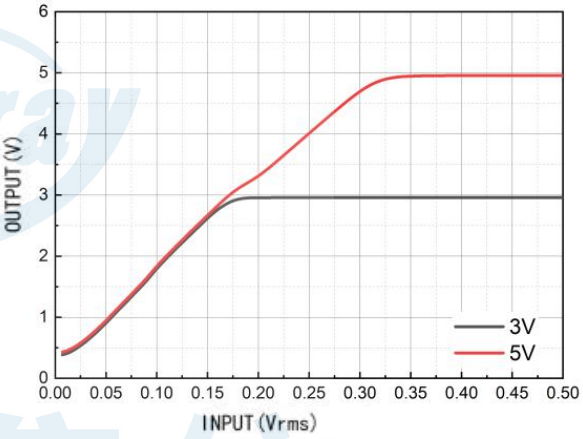
GRM Mode, input/output curves at 3V



GRM Mode, input/output curves at 5V



GRM Mode, input/output curves at 9000MHz



IRM Mode, input/output curves at 9000MHz

Circuit Principle

BR9261 uses a high-precision error amplifier to balance the output of two identical square units, thus realizing the power detection function of this product.

The BR9261 responds to the voltage of the input signal V_{IN}, producing a current squared to that voltage, which flows through the load to produce a voltage. The output is terminated by a capacitor, forming a low-pass filter whose output is the mean squared of the input V_{IN}. The filter output voltage is connected to the error amplifier, at the same time, the exact same square circuit as a negative feedback, connected to the output and input of the error amplifier, due to the high gain of the operation amplifier, the output of the two square circuits is equal, so the input of the square circuit on the feedback path (that is, the error amplifier output) is equal to the root-mean-square voltage of the input signal.

Typical Application

Figure 8 to Figure 10 is the basic circuit connection scheme of BR9261(MSOP8 package) three working modes. In each operating mode, the BR9261 requires a single Supply Voltage with a voltage range of 2.7~5.5V. Two decoupling capacitors of 100pF and 0.01μF need to be connected to the VPOS pin. When PWDN pins are connected to VPOS, the Supply Current can be reduced from 0.5mA in normal operation to 1μA.

The input should be connected to a 2.2MΩ external bypass resistor and coupling capacitor to achieve broad band approximate 50Ω impedance matching. The relationship between the input impedance and the coupling network is discussed in detail below.

The input coupling capacitance and the input resistance inside the chip together determine the corner frequency of the input:

$$f_{-3dB} = \frac{1}{2\pi C_C R_{IN}}$$

If the 100pF capacitor in Figures 8 to 10 is used, the corner frequency is about 10kHz.

The output voltage is 6.5 times that of the input signal Vrms (conversion Power Gain is 6.5V/V rms). Different operating modes can be adjusted by setting SREF and IREF. As shown in Figure 8, under the condition of 5V supply voltage, the output swing is 0.08~4.9V, and the other two modes will add different offset voltages to the output voltage.

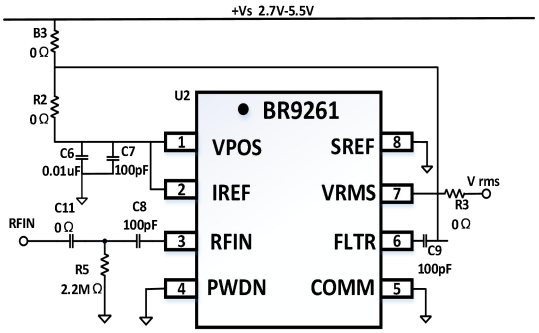


FIG. 8 GRM Mode Basic Connection Circuit Block Diagram

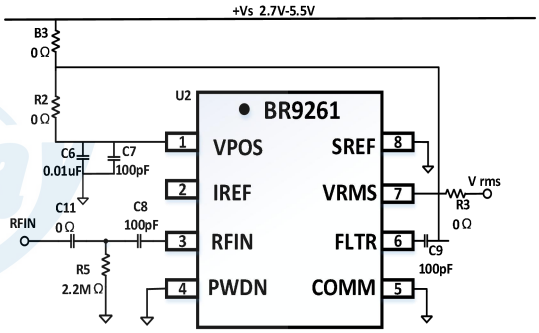


FiG. 9 Basic Connection Circuit Block Diagram of IRM Mode

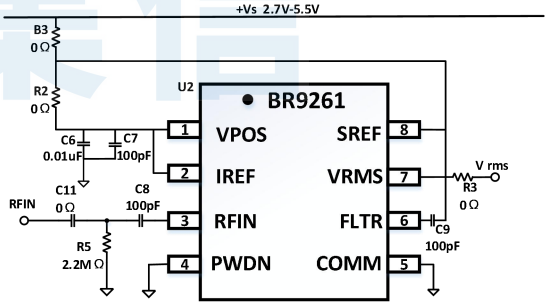


FiG. 10 Basic Connection Circuit Block Diagram of SRM Mode

In the internal reference mode (FIG. 9), the output voltage will increase the offset of 410mV@VPOS=5V. In the Power reference mode (Figure 10), the output voltage will increase the offset of 670mV@VPOS=5V. Table 3 provides a detailed Notes of the connection mode, output swing, and minimum output voltage for each operating mode.

Table 4 Operating Mode Characteristics (5V Supply Voltage)

Mode	IREF	SREF	Output (V) (no input)	Output (V)
GRM	VPOS	COMM	0.07	* V_{IN}
IRM	OPEN	COMM	0.412	* V_{IN}+0.42
SRM	VPOS	VPOS	0.66	* V_{IN}+0.66

Output Swing

FIG. 11 shows the output voltage curves of BR9261 under three operating modes under 5V operating conditions. As can be seen from the figure, both the internal reference mode and the power reference mode reduce the effective dynamic range of the device. Lowering the voltage range causes the same problem.

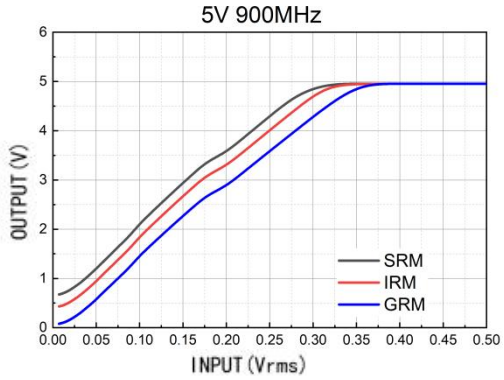


FIG. 11 Output Swing for Three Operating Modes

Dynamic Range

The BR9261 is a linear gain system with a dynamic gain of G, and the dB value of its dynamic range cannot be visually displayed in Figure 12. While the input power dB increases in steady steps, the output power grows at a rate (with dB) that increases in steps. Figure 12 illustrates the relationship between the rate of output growth (V/Vrms) and the rate of input Vrms growth.

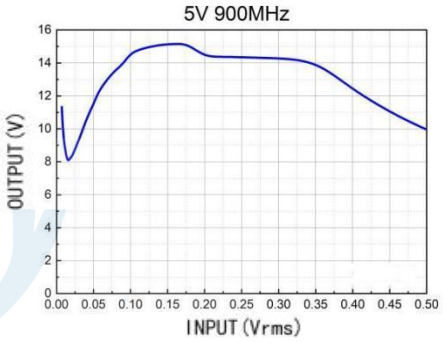


FIG. 12 Relation between Output Variation Amplitude and input Voltage

Output Coupling and Matching

There are a variety of methods for input impedance matching. For multi-frequency applications, as shown in Figure 13, 2.2MΩ bypass resistors can provide good in-band matching. For a single frequency, resonant matching can be used. The optimum value of the matching resistance can be found on the Smith original drawing. At 1GHz, the VSWR can be less than 1.5. At extremely high frequencies (1.8GHz to 2.5GHz), the VSWR may be greater than 1.5 for a bypass resistance condition. If the VSWR is strictly required, then the bypass resistance can be replaced with a series inductor, as shown in Figure 13.

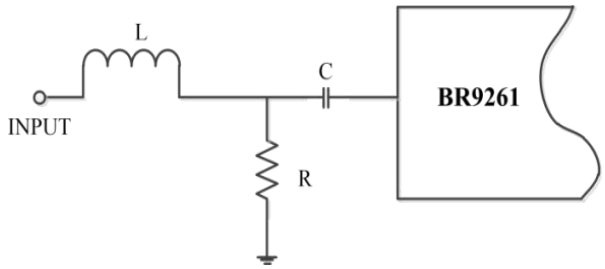


FIG. 13 Impedance Matching Network

Table 4 is a list of recommended matching resistance and inductance values for high frequency conditions. C is the isolating capacitance and has nothing to do with impedance matching.

Table 5 Impedance Matching Relationship

Frequency	L/nH	R / Ω	C/pF
2 MHZ to 2.5 GHz	-	2.2 M	100
	(Welding Capacitor)47pF	16	47

Note: 2.2M Ω matching has good response at low power input; 16 Ω matching has good stability and stability under high power input.

Power, Enable, and Power on

The static current of the BR9261 is about 0.4mA, and there is not much difference in static power consumption under different supply voltages and input amplitudes.

Users can turn off the BR9261 by connecting the PWDN (pin 4) to the VPOS or by turning off the power supply. When turned off, the chip leakage current is less than 1μA.

When the BR9261 is in the off state (PWDN=VPOS) input signal, the leakage current will increase, and the increase amplitude is related to the amplitude of the input signal.

Voltage and dBm Conversion

In many charts, the abscissa needs to be converted between Vrms voltage and dBm. In general, dBm is calculated relative to the 50Ω impedance. In a 50Ω system, the conversion between dBm and voltage can be performed using the following formula.

$$\text{Power(dBm)} = 10\lg\left[\frac{(V_{\text{rms}})^2}{\frac{50\Omega}{0.001}}\right]$$

$$= 10\lg[20(V_{\text{rms}})^2]$$

$$V_{\text{rms}} = \sqrt{0.001 \times 50\Omega \times \log^{-1}\left(\frac{\text{P(dBm)}}{10}\right)}$$

$$= \sqrt{\frac{\log^{-1}\left(\frac{\text{P(dBm)}}{10}\right)}{20}}$$

$$= ((10 \text{ ^ } (\text{P (dBm)} / 10)) / 20)) \text{ ^ } 0.5$$

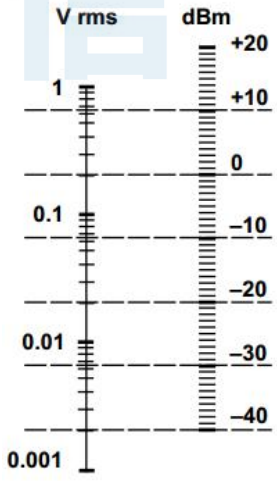


FIG. 14 The Conversion between DBM and Vrms Voltage

Output Drive Capability and Output Buffer

The BR9261 can output about 3mA of current. If a larger drive current is required, a simple output buffer circuit can be added.

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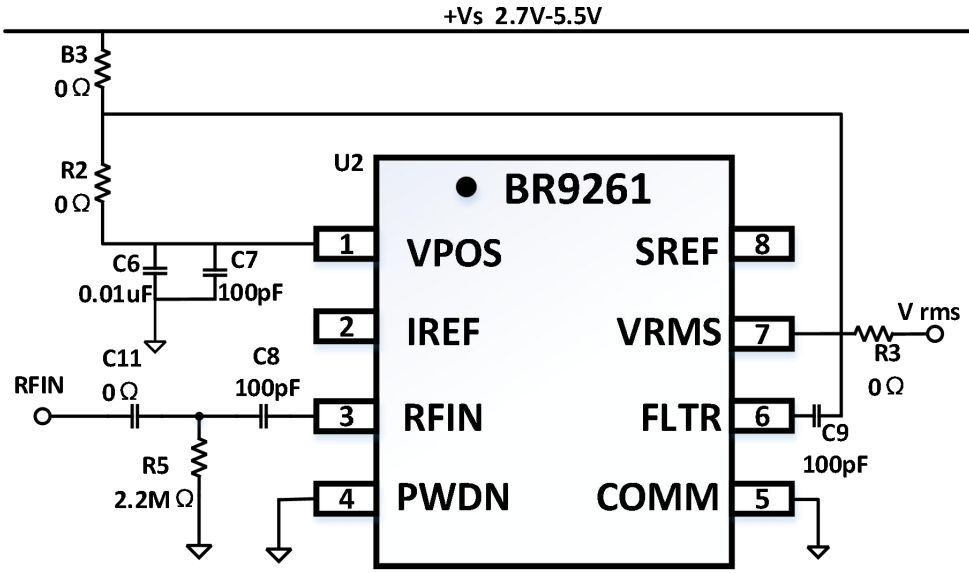
Typical Application Schematic



Bill of Material

Designator	Package	Description	Part Number
C6	0402	10nF	GRM1885C1H103JA01
C7,C8,C9	0402	100pF	GRM1885C2A101JA01
R5	0402	2.2 M Ω	RC0402JR-072M2L
R2, R3, C11	0402	0 Ω	RC0402FR-070RL
B3[2]	FB0603	220 Ω @ 100 MHZ / 2200 ma	Magnetic Bead, UPZ1608U221-2R2TF

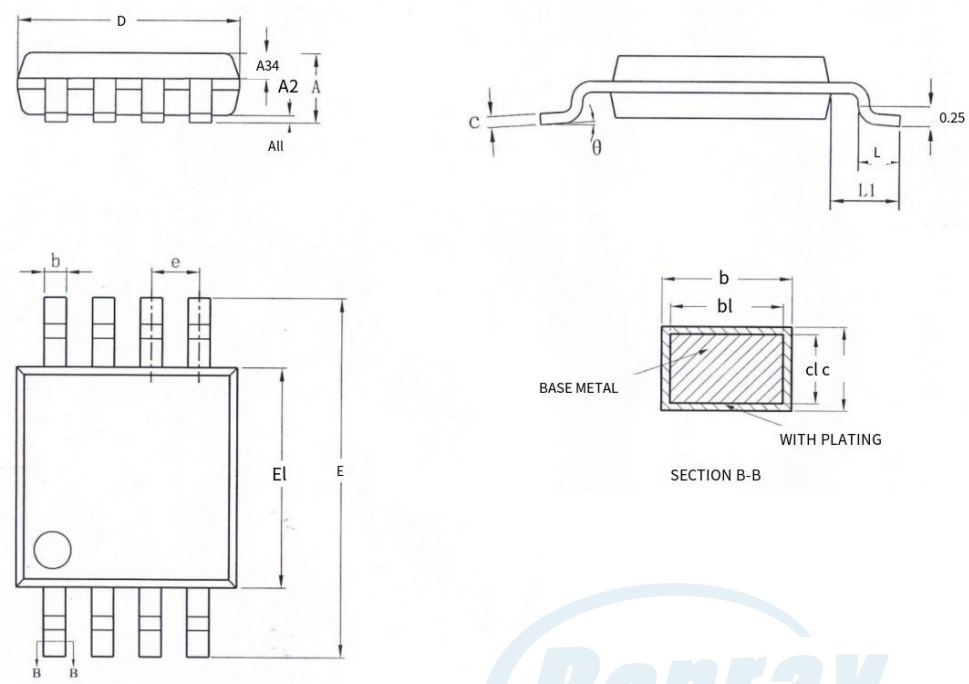
1. C11 bit number actually uses 0 ohm line to do short-circuit processing;

2. B3 bit number is recommended to use magnetic beads, which can effectively suppress the interference of the power supply, and 0 ohm line short-circuitry can also be used instead.

Refer to The Truth Table

Reference Pattern	IREF	SREF
Ground	Vs	GND
Internal	NC	GND
Supply	Vs	Vs

Package Dimensions (mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°