Product Features

Frequency: DC ~ 4GHz

Gain: 15.1dB@2.2GHz

Psat: 48.4dBm@2.2GHz

PAE: 48.6%@2.2GHz

Supply Voltage: 28V, I_{DQ} 200mA

Package: metal ceramic package

Applications

Power Amplification Stage for Wireless Infrastructure

Test and Measurement Equipment

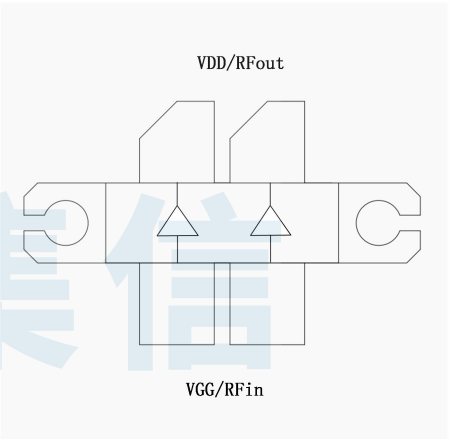
Commercial and Military Radars

Universal Transmitters and Jammers

General Description

BRGP040070PFD is a pre-matched transistor designed using the GaN HEMT process, using a +28V drain supply to achieve 70W (48.4dBm) output in the DC to 3.5GHz with, power added efficiency (PAE) >50%. The device has good high frequency characteristics, reduces the sensitivity of external matching circuit, and is convenient for users to realize high frequency and ultra-wideband schemes through external matching design. The package form is a metal ceramic package with flange, excellent thermal conductivity, and the user can choose a variety of ways to install. This product is suitable for microwave communication, radar and other fields.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGP040070PFD	PF	DC-4GHz 70W GaN Transistor

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain Current (I_D)	10A
Gate Current (I_G)	18mA
Continuous Dissipated Power (P_D)	100W
Channel Temperature (T_{CH})	225 ℃
Mounting Temperature (30 seconds)	245 ℃

Note:Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Numerical values
Drain Voltage (V_{DD})	+28V
Drain Static Current (I_{DQ})	200mA
Gate Voltage (V_{GG})	2.4 V
Channel Temperature (T_{CH})	225 ℃
Continuous Dissipated Power CW (P_D)	84W
Storage Temperature	-65℃ ~ +150℃
Operating Temperature	-55℃ ~ +85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test Conditions: DEMO board test, T_A =25℃, V_{DD} =+28V, I_{DQ} =200mA, Fre=2.2GHz, CW wave, P_{out}=70W ;

Thermal Parameters

Parameters	Test Conditions	Value	Units
Thermal resistance (θ_{JC})	DC at 85 ° C case	3.3	℃/W
Channel temperature (T_{ch})		225	℃

Note: θ_{JC} to measure the thermal resistance to the bottom of the package;

ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

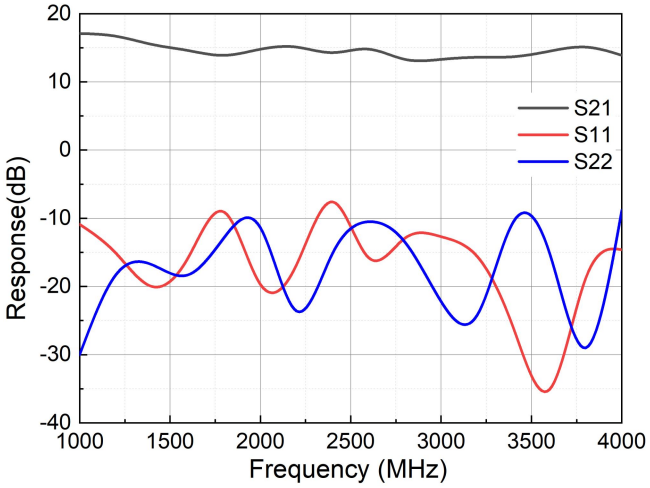
Typical Performance (EVB test data, 1GHz ~ 4GHz)

Parameters	Typ.								Units
Frequency	1000	1200	1400	1600	1800	2000	2200	2400	MHz
Gain	17.1	16.7	15.5	14.6	13.9	14.8	15.1	14.3	dB
Small Signal Input Rerurn Loss	-10.9	-15.1	-20.0	-15.8	-9.1	-19.7	-16.8	-7.6	dB
Drain Current @P_{sat}	3.890	3.520	2.454	2.120	2.675	3.640	4.760	3.806	A
Output Power @P_{sat}	47.9	47.4	46.3	45.4	45.3	46.8	48.4	47.1	dBm
Power Gain @P_{sat}	14.3	14.1	11.9	10.6	9.6	11.0	11.3	10.2	dB
PAE@P_{sat}	54.51	54.33	58.75	53.45	40.28	43.23	48.62	43.53	%
Parameters	**Typ.**								**Units**
Frequency	2600	2800	3000	3200	3400	3600	3800	4000	MHz
Small Signal Gain	14.8	13.3	13.3	13.6	13.7	14.5	15.1	13.9	dB
Small Signal Input Return Loss	-15.8	-12.9	-12.7	-15.6	-26.1	-35.1	-18.8	-14.6	dB
Drain Current @P_{sat}	4.477	4.841	4.660	4.722	4.520	5.220	4.460	3.670	A
Output Power @P_{sat}	47.0	46.8	47.8	48.2	46.9	47.8	47.9	46.5	dBm
Power Gain @P_{sat}	11.0	9.5	9.7	9.5	10.1	10.7	11.6	11.7	dB
PAE@P_{sat}	36.81	31.35	41.23	44.36	34.92	38.15	45.96	40.53	%

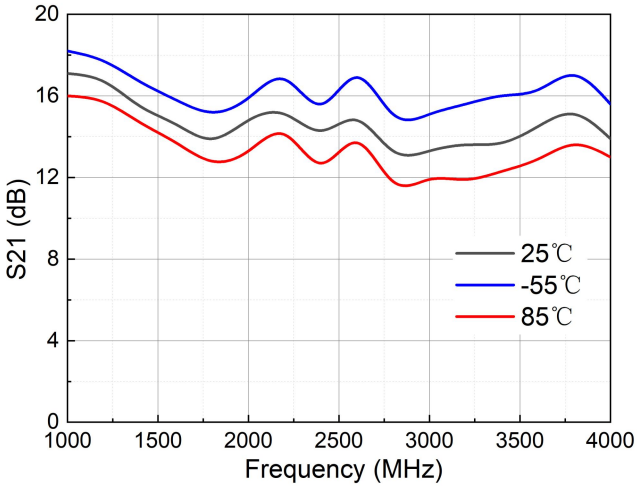
Test Conditions: Temp =+25℃V_{DD}, =+28V, =I_{DQ}200mA, CW ;

Note: P_{sat} defined as the saturation power output by the evaluation board;

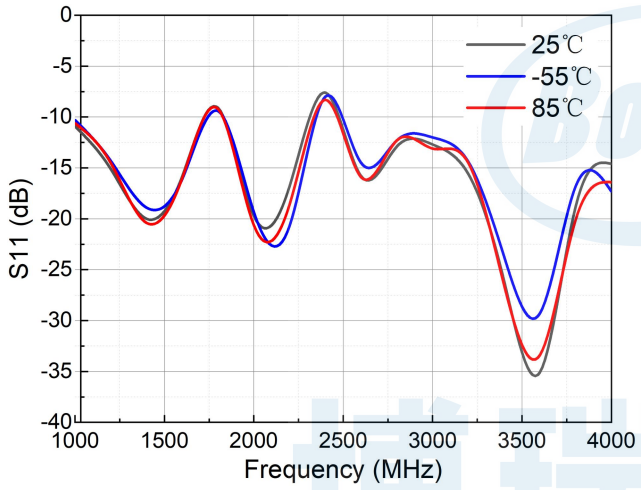
Typical Performance (Evaluation board: 1GHz~4GHz, Temp =+25℃, V_{DD}=+28V, I_{DQ}=200mA, CW wave test)



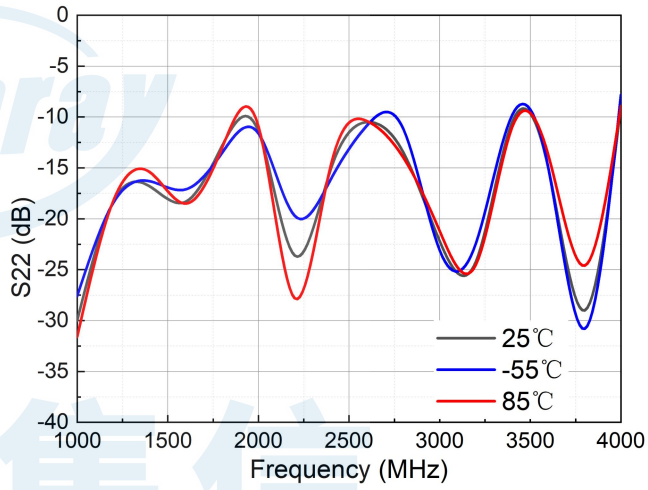
Gain & Return Loss vs. Freq



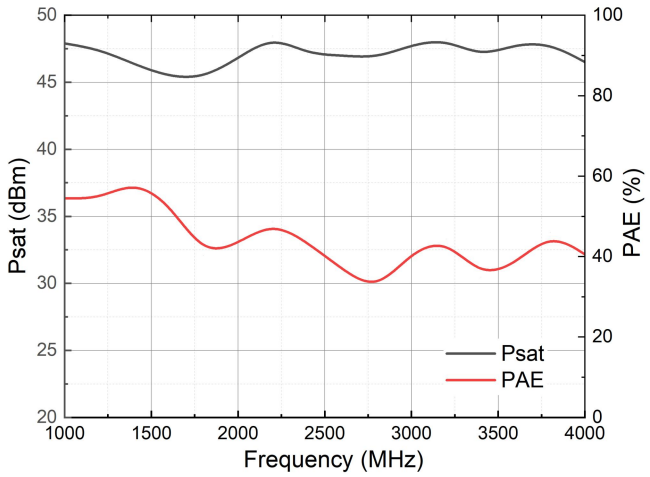
Gain vs. Freq



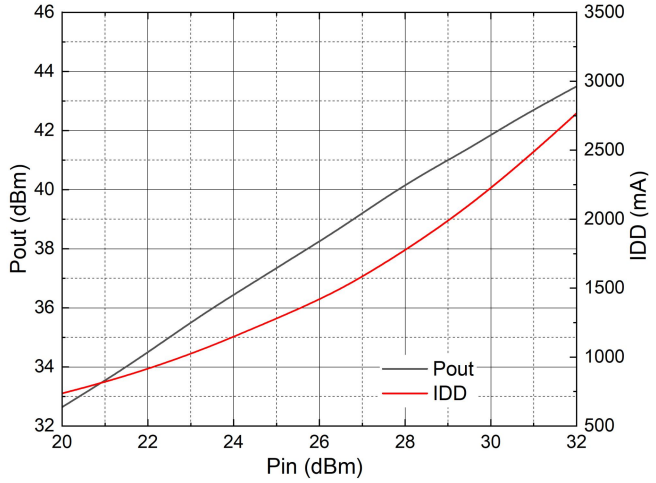
Input Return Loss vs. Freq



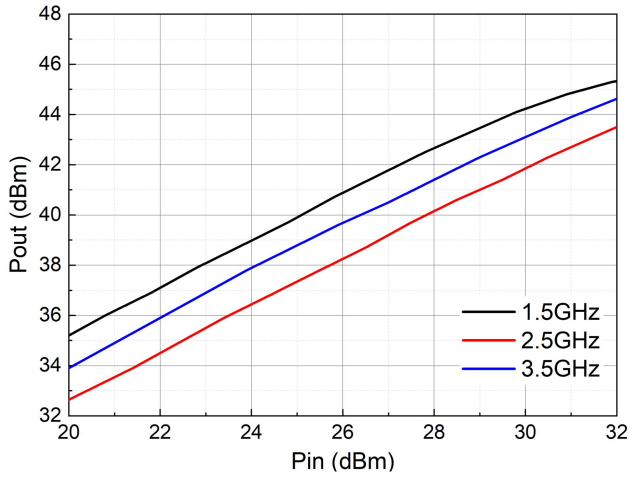
Output Return Loss vs. Freq



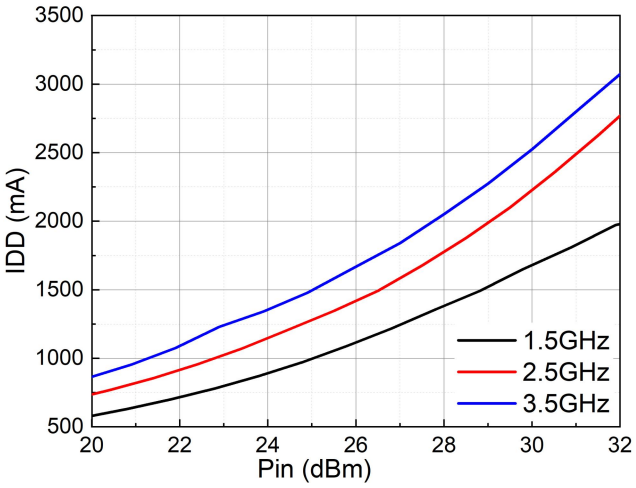
Psat vs. Freq



P_{out} & IDD vs. P_{in} @2.5GHz

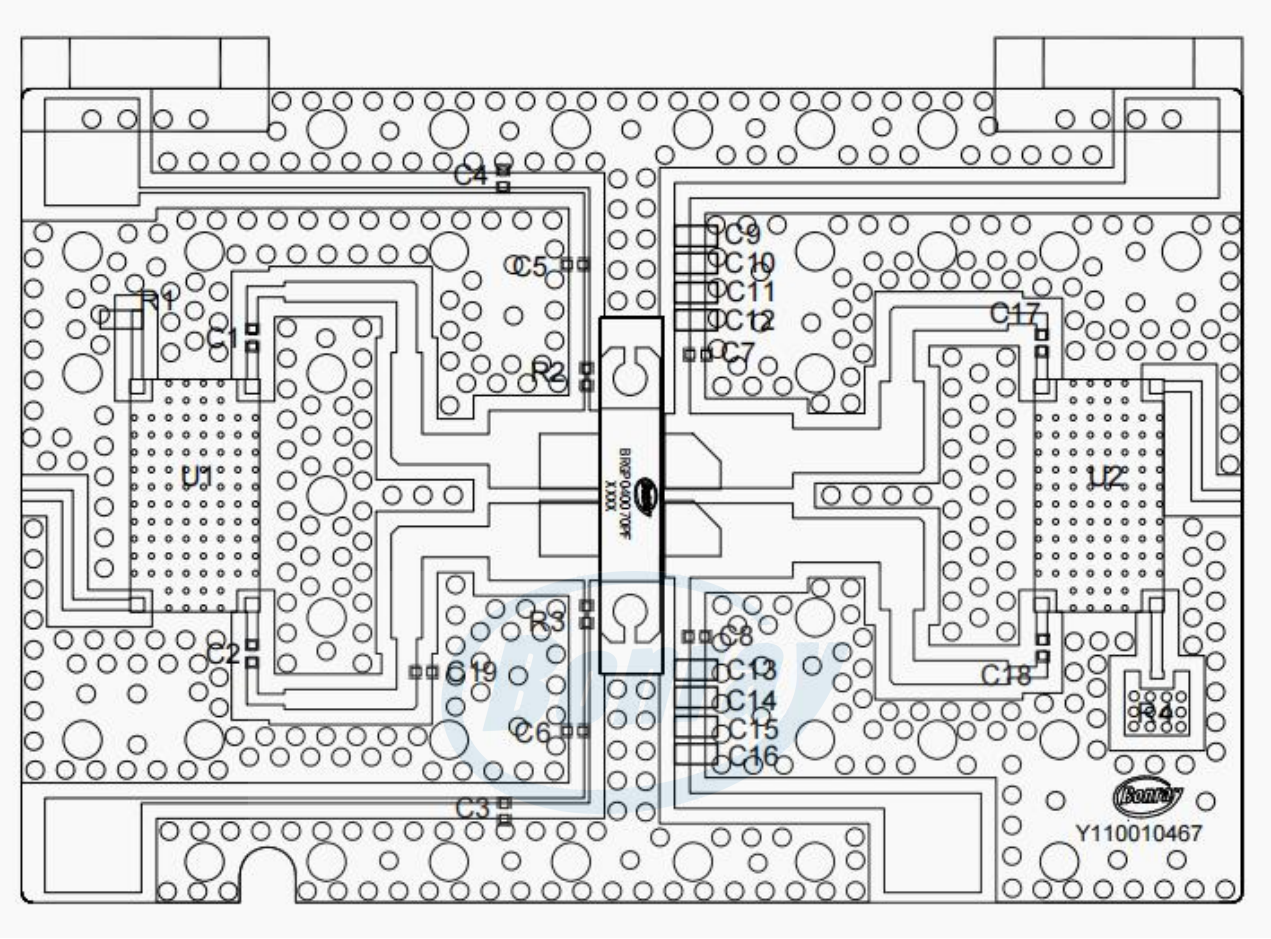


P_{out} vs. P_{in}



IDD vs. Pin

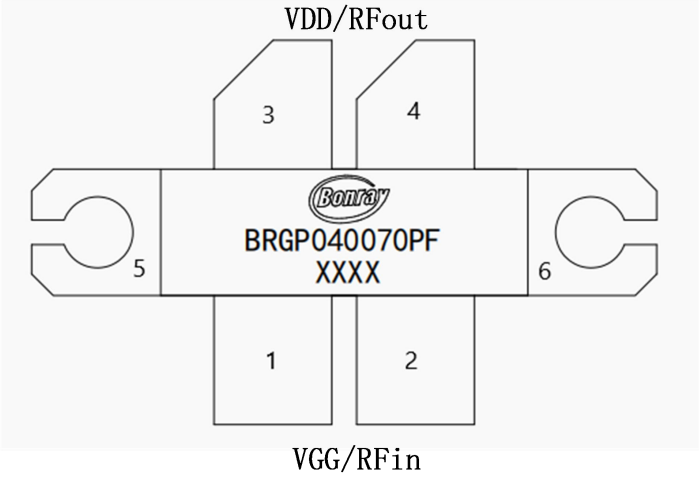
PCB Evaluation Board



Bill of Material

Designator	Package	Description	Part Number
C1, C2, C5, C6	603	15pF	GQM1875C2E150FB12#
C3, C4	1210	47uF	GRM32ER61C476KE15L
C7, C8	805	100pF	VJ0805D101JXPAJ
C17, C18	603	12pF	GQM1875G2E120FB12#
R1	SMT	50Ω, RFR50-20CT0421B	RFR50-20CT0421B
R2, R3	603	10 Ω	RC0603FR-0710RL
R4	SMT	50Ω, RFT50-100CT6363	RFT50-100CT6363
U1, U2	/	1 to 4GHz; 3dB bridge	HC2600W03
C9, C10, C11, C12, C13, C14, C15, C16	1210	CAP,10uF,100VDC,C1210	GRM32EC72A106KE05

Pin Configuration and Description



Pin Number	Pin Name	Description
1, 2,	VGG/RFin	Gate voltage / RF Input matched to 50 ohms;
3, 4	VDD/RFout	Drain voltage / RF Output matched to 50 ohms;
5 or 6	Package Base	Source connected to ground;

Power-on Sequence

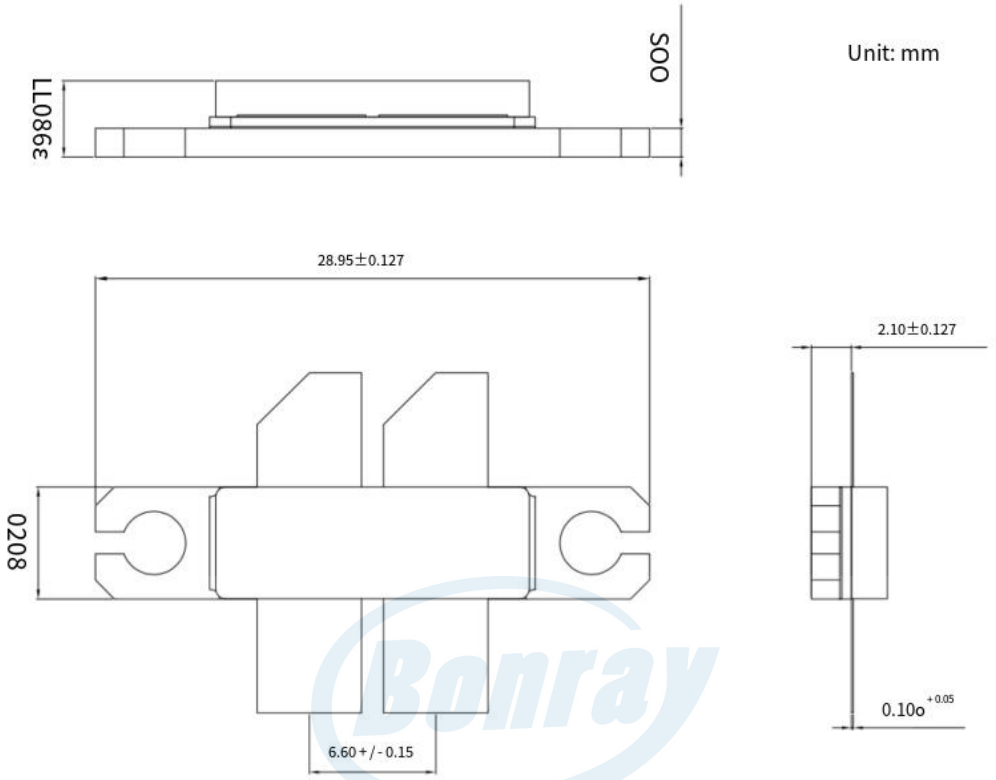
1. Set the gate voltage (V_{GG}) to -5V;
2. Set drain voltage (V_{DD}) to +28V, current limit 5A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 200mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal;
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off drain supply voltage;
4. Turn off the gate supply voltage;

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



Recommended Soldering Temperature Profile