Product Features

Frequency: DC ~ 4GHz

Gain : 15.7dB@2.0GHz

Psat: 47.6dBm@2.0GHz

PAE: 52.7% (2.0GHz,Pout=47.6dBm)

Operation Voltage: 28V, I_{DQ}300mA

Package: PC (ceramic seal)

Applications

Power Amplification Stage for Wireless Infrastructure

Test and Measurement Equipment

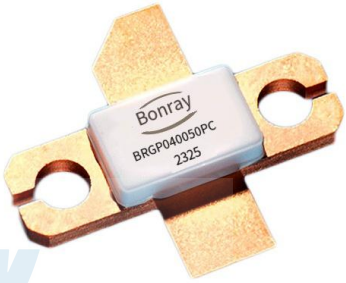
Commercial and Military Radars

Universal Transmitters and Jammers

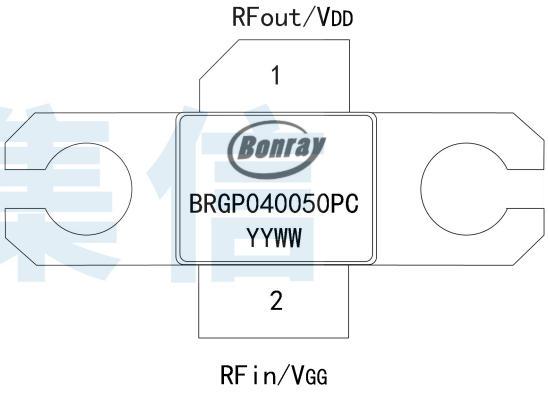
Ultrashort Wave Communication Equipment

General Description

The BRGP040050PC pre-matched transistor designed using the GaN HEMT process, using a +28V drain supply to achieves 50W (47dBm) output in the DC to 4GHz with a power add efficency (PAE) > 50%.This power amplifier has the characteristics of high efficiency, high gain and wide bandwidth. Its input terminal adopts pre-matching design, has good high frequency characteristics, reduces the sensitivity of external matching circuit, and is convenient for users to realize high frequency and ultra-wide band schemes through external matching design. The package form is a metal ceramic package with flange, excellent thermal conductivity, and the user can choose a variety of ways to install. This product is suitable for microwave communication, radar and other fields.



Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGP040050PC	PC	DC ~ 4GHz 50W GaN Transistor

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain Current (I_D)	6A
Gate Current (I_G)	14mA
Continuous Dissipated Power (P_D)	75W
Channel Temperature (T_{CH})	275 °C
Mounting Temperature (30 seconds)	245 °C

Note: Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Values
Drain Voltage (V_{DD})	+28V (Typ)
Drain Static Current (I_{DQ})	300mA (Typ)
Gate Voltage (V_{GG})	-2.63V (Typ)
Channel Temperature (T_{CH})	225 ° C (Max)
Continuous Dissipated Power CW (P_D)	60W (Max)
Storage Temperature	-65℃ ~ +150℃
Operating Temperature	-55℃ ~ +85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test Condition: DEMO board test, T_A =25℃, V_{DD}=+28V,I_{DQ}=300mA, Fre=1GHz, CW , P_{out}=50W;

Thermal Parameters

Parameters	Test Conditions	Value	Units
Thermal Resistance (θ_{JC})	DC at 85 ° C case	3.3	℃/W
Channel Temperature (T_{ch})		225	℃

Note: θ_{JC} to measure the thermal resistance to the bottom of the package;

ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

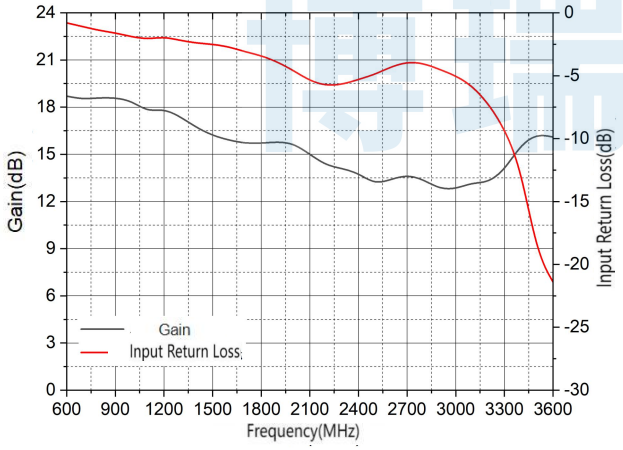
OBSERVE HANDLING PRECAUTIONS

Typical Performance (Evaluation Board)

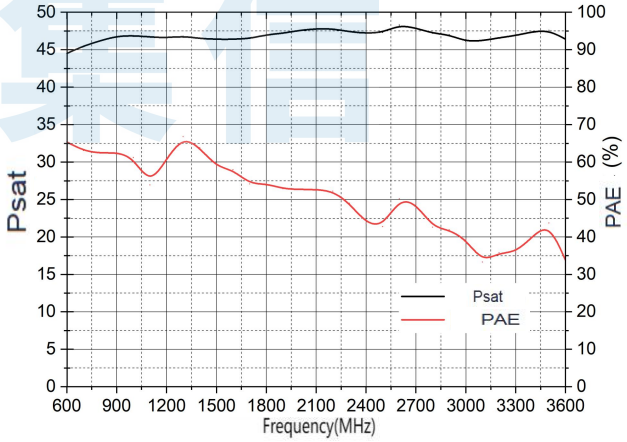
Evaluation Board (0.6GHz-3.6GHz) Test Data							
Parameters	**Typ.**						**Units**
Frequency	700	1000	1500	2000	3000	3500	MHz
Gain	18.5	18.4	16.2	15.7	12.8	16.3	dB
Small Signal Input Return Loss	-1.1	-1.9	-2.5	-4.6	-5.0	-19.1	dB
Drain Current @P_{sat}	1.89	2.67	2.42	3.44	3.25	4.14	A
Pout (dBm) @P_{sat}	45.5	46.9	46.4	47.6	46.1	47.6	dBm
Pout (dBm) @P_{sat}	35.3	48.6	43.7	57.3	40.9	58.0	W
PAE@P_{sat}	63.1	61.2	58.7	52.7	39.3	43.7	%
Power Gain @P_{sat}	12.6	12.2	10.8	9.4	9.0	9.0	dB
Test Condition: Temp =+25℃, V_{DD}=+28V, I_{DQ}=300mA, CW;							

Note: P_{sat} defined as the maximum power output by the evaluation board;

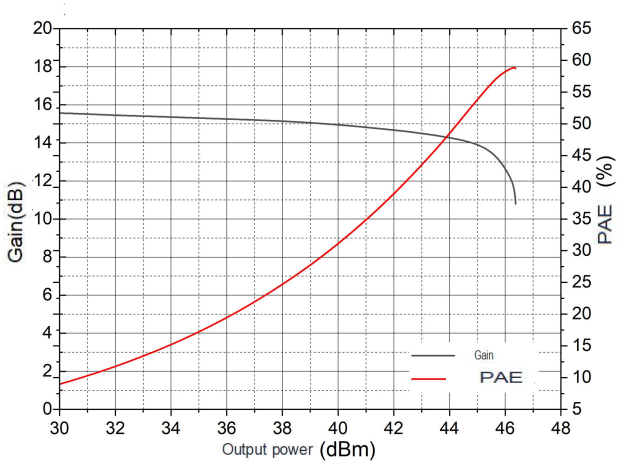
Typical Performance (Evaluation Board: 0.6GHz-3.6GHz, Temp =+25℃, V_{DD}=+28V, I_{DQ}=300mA, CW wave test)



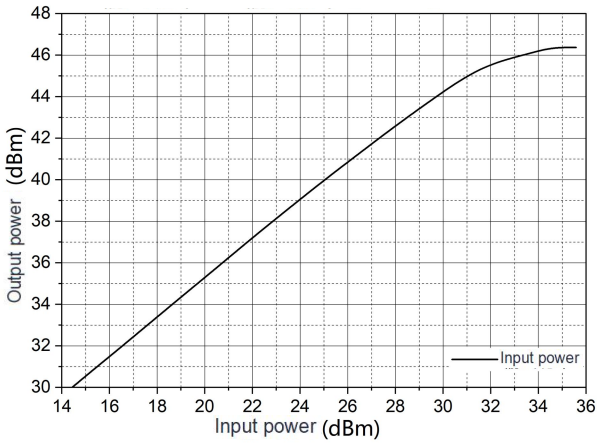
Standing Wave, Gain vs. Freq@25℃



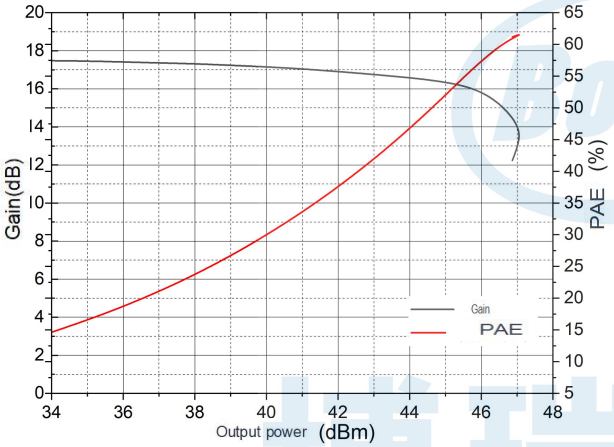
Gain,Psat,PEA vs. Freq@25℃



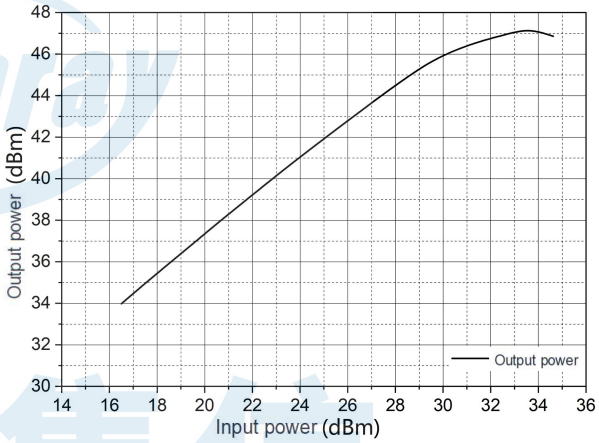
Gain, PEA vs. P_{out} @1.5GHz



P_{out} vs. P_{in}@1.5GHz

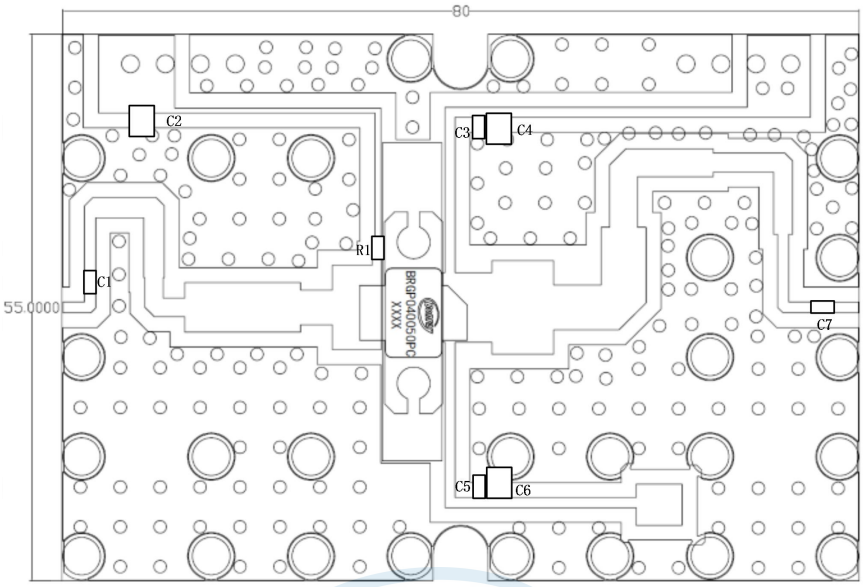


Gain, PEA vs. P_{out} @1GHz



P_{out} vs. P_{in}@1GHz

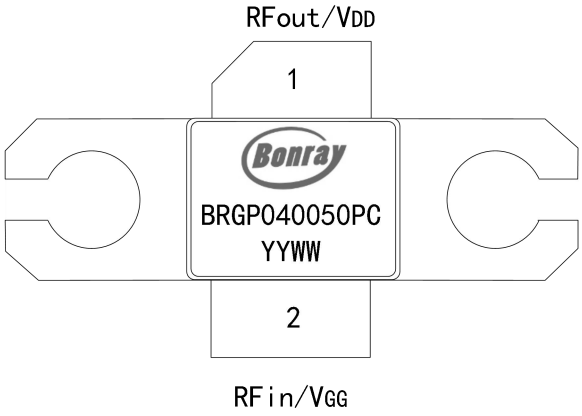
PCB Evaluation Board



Bill of Material

Designator	Package	Description	Part Number
U1	PC	50W pre-matched transistor	BRGP040050PC
C1	0603	15pF	GQM1875C2E150FB12#
C7	0603	47pF	GQM1875C2E470FB12#
C3,C5	0603	27pF	GQM1875C2E270FB12#
R1	0603	51 Ω	RC0603FR-0751R1L
C2,C4,C6	1210	10uF	GRM32EC72A106KE05

Pin Configuration and Description



Pin Number	Pin Name	Description
1	RFout/V_{DD}	Drain voltage / RF Output matched to 50 ohms;
2	RFin/V_{GG}	Gate voltage / RF Input matched to 50 ohms;
-	Package Base	Source connected to ground;

Power-on Sequence

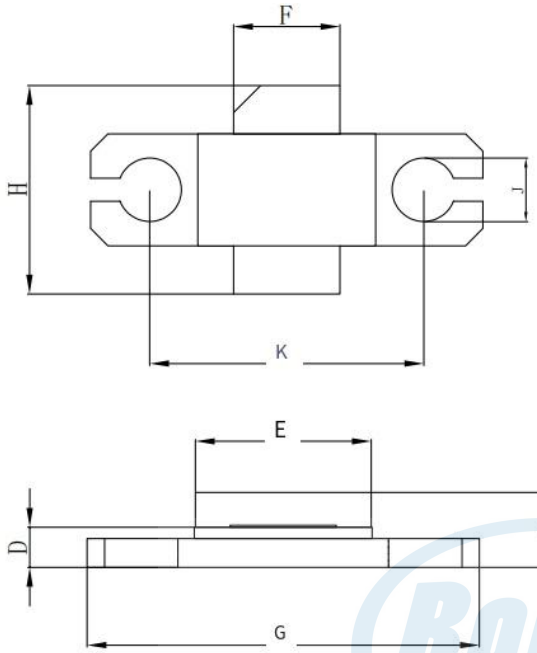
1. Set the gate voltage (V_{GG}) to -5V;
2. Set drain voltage (V_{DD}) to +28V, current limit 8A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 300mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal;
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off drain supply voltage;
4. Turn off the gate supply voltage;

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



DIM	Units : mm MIN	MAX
A	5.67	5.93
B	0.05	0.15
C	3.18	4.19
D	1.93	2.23
E	9	9.2
F	5.37	5.63
G	20.17	20.43
H	10.3	11.3
J	3.3±0.13	
K	14.2±0.13	

Recommended Soldering Temperature Profile