Features

Frequency: DC ~ 6GHz

Gain: 17.3dB@900MHz

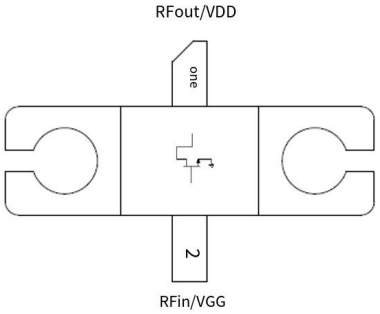
P_{sat}: 44.7dBm@900MHz

PAE: 62.4%(Pout=44.7dBm, 900MHz)

Operation Voltage:28V, static current 320mA

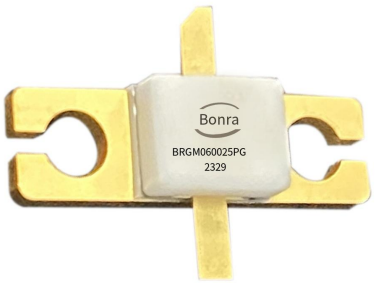
Package: PG (ceramic)

Functional Block Diagram



General Description

The BRGM060025PG is a Gallium nitride (GaN) wideband transistor with a +28V drain supply that achieves 25W (44dBm) of power output in a power added efficiency (PAE) up to 62.4%. This transistor uses the GaN process, which has the characteristics of high efficiency, high gain and wide bandwidth. This makes the product has a strong application ability in both linear and compressed amplifier circuits, and also simplifies link design and related heat consumption management.



Ordering Information

Part	Package	Description
BRGM060025PG	PG	DC ~ 6GHz GaN Transistor

Absolute Maximum Ratings

Parameters	Values
Gate drain breakdown voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain current (I_D)	5.1 A
Gate current (I_G)	9mA
Continuous power dissipation (P_D)	50W
Channel temperature (T_{CH})	275 ℃
Mounting temperature (30 seconds)	245 ℃

Note: Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Working Conditions

Parameters	Values
Drain voltage (V_{DD})	+28V (Typ)
Drain static current (I_{DQ})	320mA (Typ)
Gate voltage (V_{GG})	-2.52V (Typ)
Channel temperature (T_{CH})	225 ° C (Max)
Continuous dissipated power CW (P_D)	42W (Max)
Storage temperature	-65℃ ~ +150℃
Operating temperature	-55℃ ~ +85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test conditions: DEMO board test, =T_A25℃, V_{DD}=+28V, I_{DQ}=320mA, Freq=1GHz, CW wave, =25W test;P_{out}

Thermal Parameters

Parameters	Test Conditions	Value	Units
Thermal resistance (θ_{JC})	Dc bias Test at 85 ° C	3.3	℃/W
Channel temperature (T_{ch})		225	℃

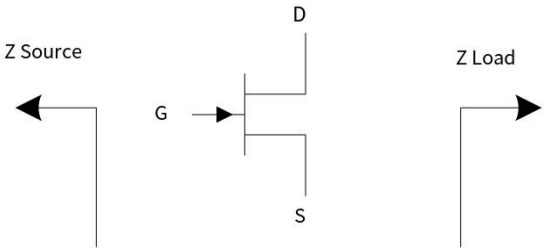
Note: To measure the thermal resistance to the bottom of the tube housing;θ_{JC}

ESD Warnings

ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

Radio Frequency Features



Optimum Power Matching

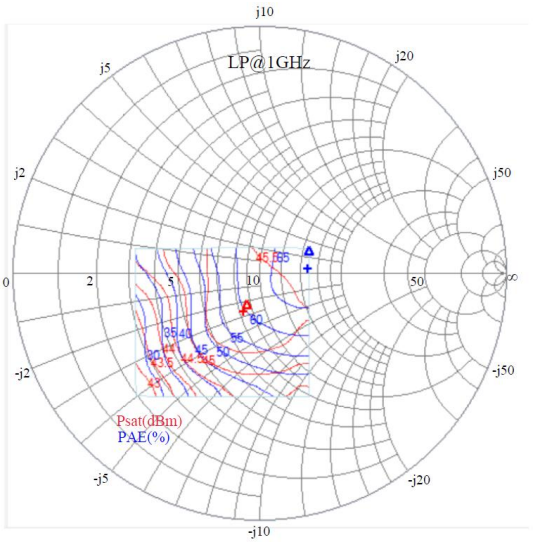
Load Pull Data -- Optimum Power Matching							
Parameters	**Typ.**						**Units**
Frequency	1000	2000	3000	4000	5000	6000	MHz
Z_{source}	2.21 + j * 5.3	1.34 * 3.93 j	3.48 * 6.53 j	2.82 * 13.95j	2.08 * 16.72j	0.15 * 25.65 j	Ω
Z_{load}	6.08 * 4.6 j	5.79 * 2.4 j	5.07 * 5.89 j	5.1 * 9.58 j	4.24 * 15.86j	14.64 * 20.75 j	Ω
I_D@P_{sat}	3.13	2.41	2.19	2.8	2.63	2.9	A
OutputP_{sat}	47.34	46.15	46.05	47	46.5	47	dBm
PAE@P_{sat}	60.97	59.9	61.79	64	62	60.8	%
Gain @P_{sat}	19.13	16.94	12.24	13.6	12.3	10.1	dB
Test conditions: Temp=+25℃, =+28V, =320mA, CW wave test;$V_{DD}I_{DQ}$							

Optimum Efficiency Matching

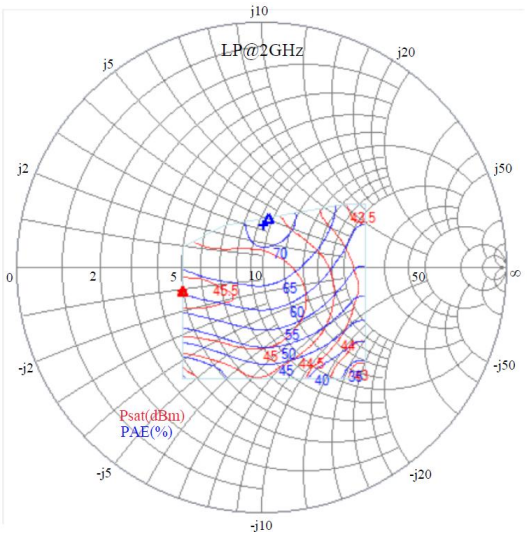
Load Pull Data -- Best Efficiency Matching							
Parameters	**Typ.**						**Units**
frequency	1000	2000	3000	4000	5000	6000	MHz
Z_{source}	2.21 + j * 5.3	1.34 * 3.93 j	3.48 * 6.53 j	2.82 *13.95 j	2.08* 16.72j	0.15 * 25.65 j	Ω
Z_{load}	14.63+j *3.08	10.44+j*5.83	4.51 * 3.13 j	3.85 * 7.42 j	4.2 * 12.76 j	14.64 * 20.75 j	Ω
I_D@P_{sat}	1.55	1.16	1.5	1.22	1.65	2	A
OutputP_{sat}	44.88	43.81	44.99	44.06	45.03	46	dBm
PAE@P_{sat}	70.07	72.32	69.87	74	69.2	66.3	%
Gain @P_{sat}	20.27	16.8	11.76	9.8	10	9.4	dB
Test conditions: Temp =+25℃, =+28V, =320mA, CW wave test;$V_{DD}I_{DQ}$							

Load Pull Smith

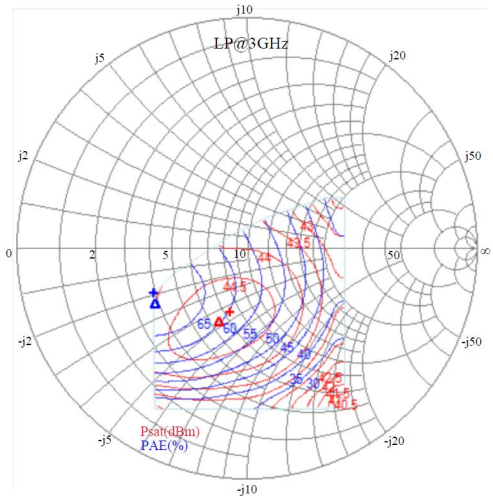
RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.



High Impedance Circle Diagram of 1GHz



High Impedance Circle Diagram of 2GHz

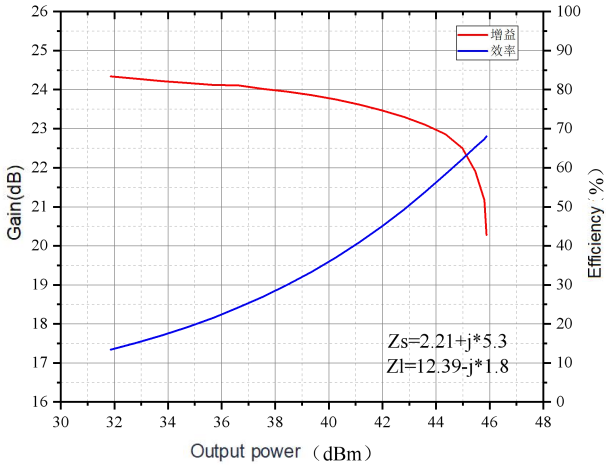


High Impedance Circle Diagram of 3GHz

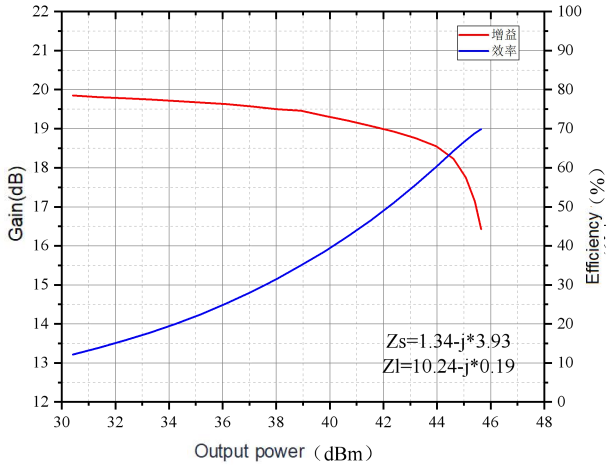
Note:

1. The central impedance of the Smith circle diagram above is Zo=10Ω;
2. The contour interval of the red line Pout in the Smith circle diagram is 0.5dB, and the PAE interval is 5%;
3. The test conditions are as follows: Temp =+25℃, V_{DD}=28V, I_{DQ}=320mA, CW wave test;

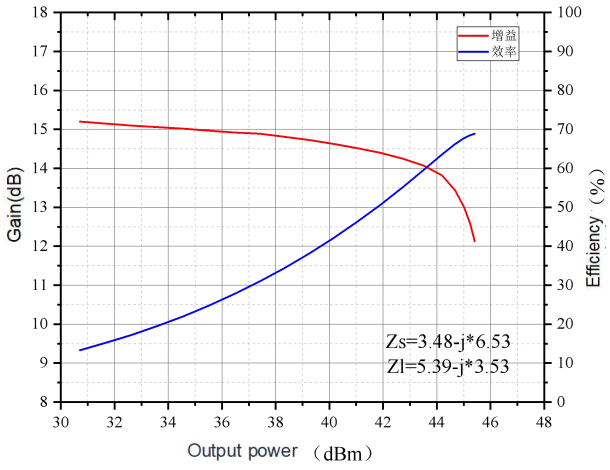
Typical Performance (Load Pull data, Temp =+25℃, V_{DD}=+28V, I_{DQ}=320mA, CW wave test)



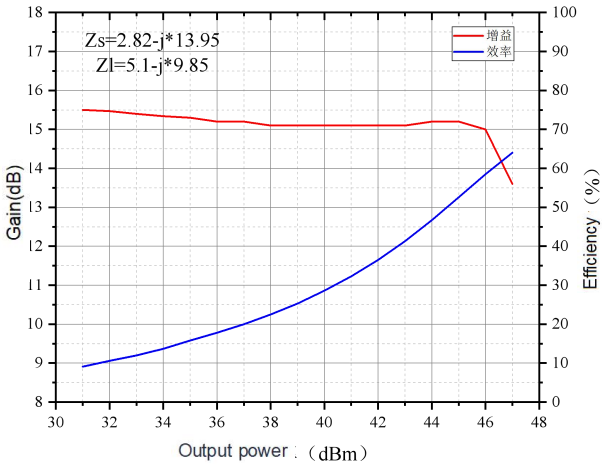
Gain, Efficiency vs P_{out}@1GHz



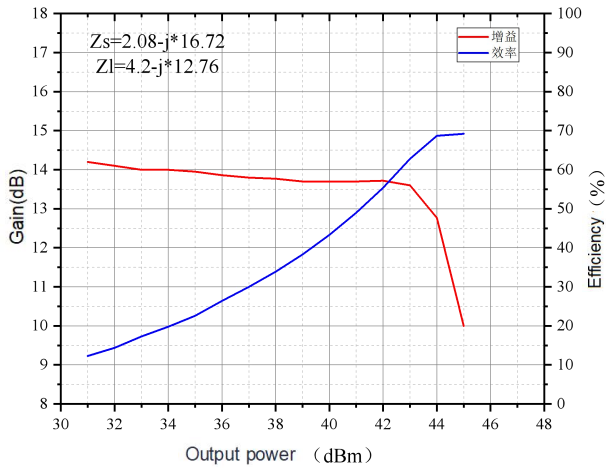
Gain, Efficiency vs P_{out}@3GHz



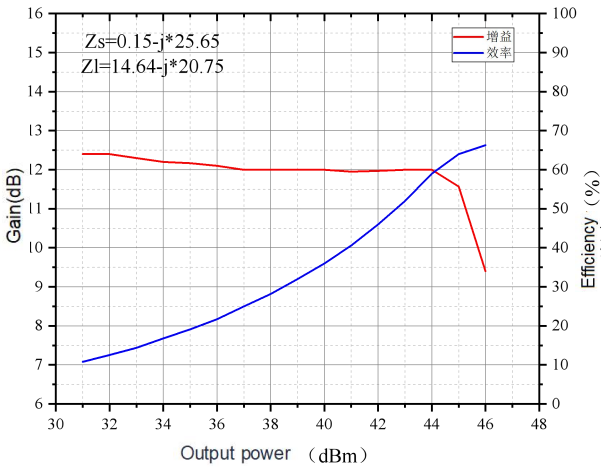
Gain, Efficiency vs P_{out}@3GHz



Gain, Efficiency vs P_{out}@4GH



Gain, Efficiency vs P_{out}@5GHz



Gain, Efficiency vs P_{out}@6GHz

Typical Performance (Performance measured in Evaluation Board)

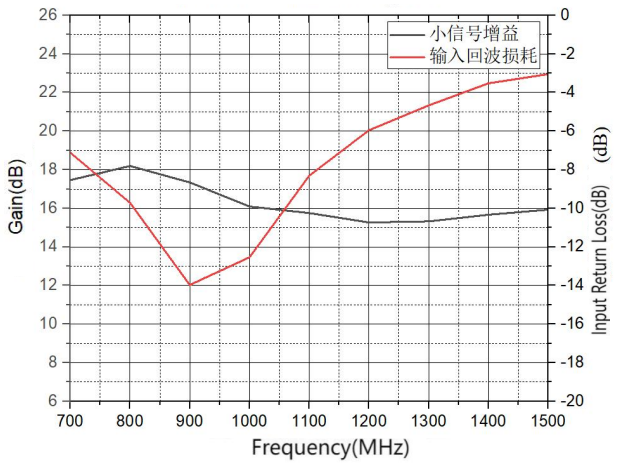
Evaluation Board (0.7GHz ~ 1.5GHz) Test Data										
Parameters	**Typ.**									**Units**
Frequency	700	800	900	1000	1100	1200	1300	1400	1500	MHz
Gain	17.5	18.2	17.3	16.1	15.8	15.3	15.3	15.7	15.9	dB
Input echo	-7.1	-9.7	-14.0	-12.5	-8.3	-6.0	-4.7	-3.5	-3.0	dB
Drain current @Psat	1.52	1.39	1.58	1.48	1.35	1.36	1.52	1.79	2.03	A
Output power @Psat	44.7	44.1	44.7	43.9	44.2	43.7	44.4	44.4	44.4	dBm
Output power @Psat	29.5	25.7	29.5	24.5	26.3	23.4	27.5	27.5	27.5	W
PAE@Psat	65.6	62.5	62.4	55.6	63.4	56.3	59.6	54.7	48.6	%
Gain @Psat	12.6	12.2	12.7	11.9	10.6	10.6	11.3	10.7	11.1	dB
Test conditions: Temp =+25℃, =+28V, =320mA, CW test;$V_{DD}I_{DQ}$										

Note: defined as the maximum power output by the evaluation board;P_{sat}

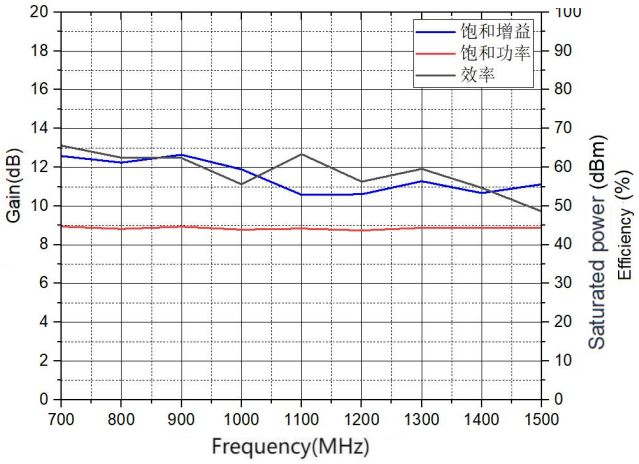
Wide Voltage Features (Evaluation Board Data)

Evaluation Board (0.7GHz ~ 1.5GHz) Test Data					
Parameters	**Typ.**				**Units**
Frequency	700	1000	1300	1500	MHz
Output power @P_{sat}	45.8	44.9	45.7	45.5	dBm
Output power @P_{sat}	38.1	30.8	37.0	35.7	W
Drain current @P_{sat}	1.79	1.69	1.76	2.25	A
PAE@P_{sat}	66.4	57.1	65.7	49.6	%
Gain @P_{sat}	12.68	11.86	10.61	10.36	dB
Test conditions: Temp =25℃, =+32V, =320mA, CW test;$V_{DD}I_{DQ}$					

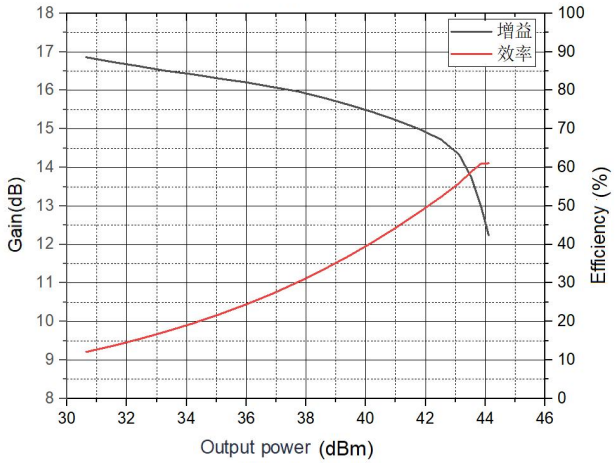
Typical Performance (evaluation board: 0.7GHz ~ 1.5GHz, Temp =+25℃, V_{DD} =+28V, I_{DQ}=320mA, CW wave test)



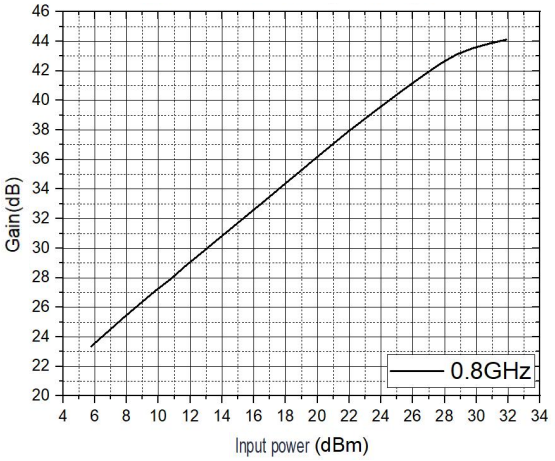
Standing Wave, Gain vs Freq



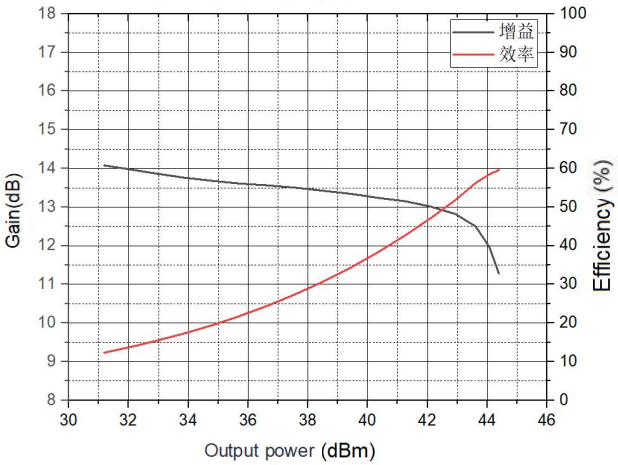
Saturated Power, Gain vs Freq



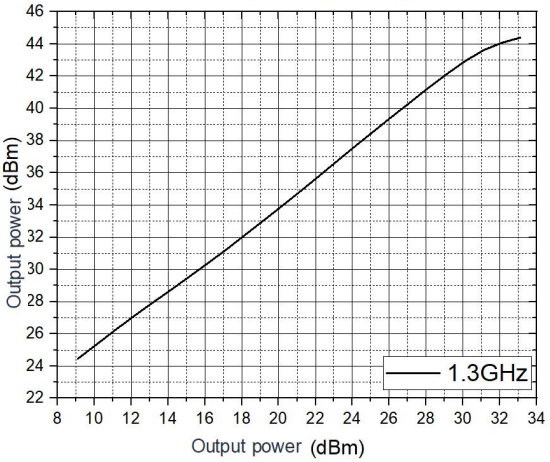
Gain, Efficiency vs P_{out}@0.8GHz



Pin vs P_{out}@0.8GHz

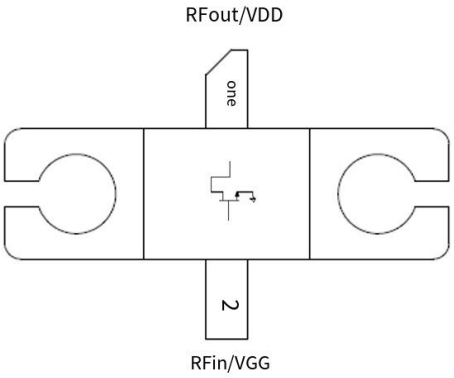


Gain, Efficiency vs P_{out}@1.3GHz



Pin vs P_{out}@1.3GHz

Pin Configuration and Description



Pin Number	Pin Name	Description
1	RFout/V_{DD}	Drain voltage / RF Output matched to 50 ohms;
2	RFin/V_{GG}	Gate voltage / RF Input matched to 50 ohms;
-	Package Base	Source connected to ground;

Power-on Sequence

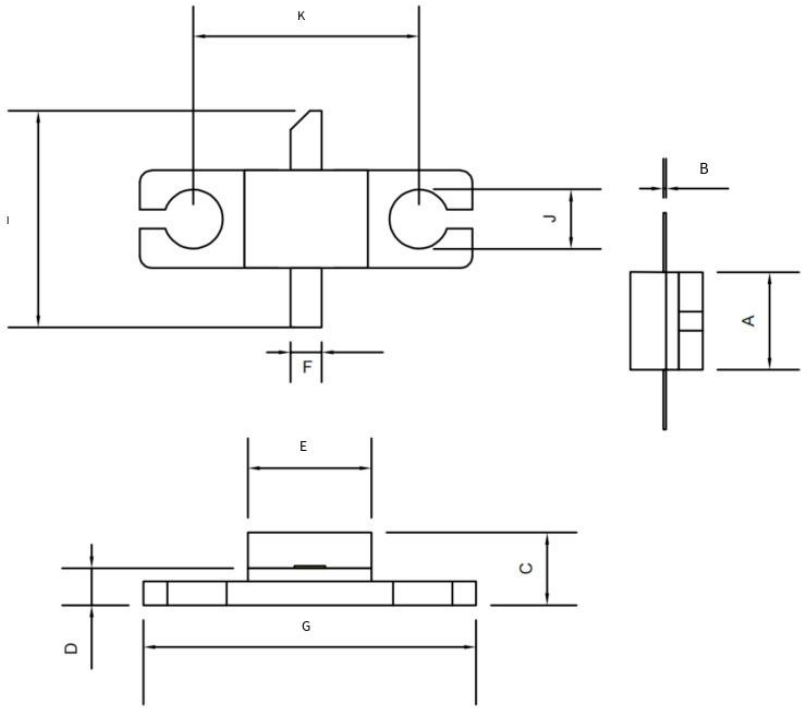
1. Set the grid voltage (V_{GG}) to -5V
2. Set drain voltage (V_{DD}) to +28V, current limit 5A;
3. Turn on the grid voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 320mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal;
2. Reduce the grid voltage (V_{GG}) to -5V;
3. Turn off drain supply voltage;
4. Turn off the grid supply voltage;

Note: When the circuit is designed, the offset voltage needs to have a timing protection circuit to ensure that it is fully powered on before adding, and ensure that it is reduced to below 5V when powering off, before starting to power off; $V_{GG}V_{DD}V_{DD}V_{GG}$Especially in TDD applications, grid supply decoupling capacitors need to be rigorously evaluated to meet the switching speed requirements.

Package Dimensions (mm)



Unit: mm

Dim	Min	Typ	Max
A	4	4.1	4.2
B	0.05	0.1	0.15
C	2.9	3.15	3.4
D	1.4	1.55	1.7
E	5.05	5.2	5.35
F	1.25	1.3	1.35
G	13.9	fourteen	14.1
H	9.7	10	10.3
J	2.42	2.5	2.58
K	9.45	9.5	9.55

Recommended Soldering Temperature Profile