Product Features

Frequency: 2GHz ~ 6GHz

Gain: 26.6dB@2GHz

Psat: 41.2dBm@2GHz

PAE: 49.1%@2GHz

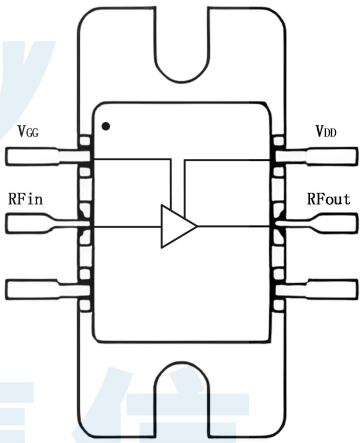
V_{DD}Power Supply 28V, static current 350mA

Package: PH (metal package)

General Description

BRGF060010PHG is an internally matched ultra wideband power amplifier designed based on GaN process. The product covers the frequency range of 2GHz ~ 6GHz, using +28V drain power supply, quiescent current 350mA, input and output impedance has been matched to 50Ω, with good high frequency characteristics, reduce the sensitivity of external matching circuit, easy for users to achieve high frequency and ultra-wideband solutions through external matching design.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGF060010PHG	PH	2GHz to 6GHz Internal Matched PA

Absolute Maximum Ratings

Parameters	Values
Gate drain breakdown voltage (BV_{DG})	100V
Gate pressure range (V_{GG})	-6 to 0V
Drain current (I_D)	1.8 A
Gate current (I_G)	8mA
Continuous dissipated power (P_D)	35W
Channel temperature (T_{CH})	275 ℃
Mounting temperature (30 seconds)	245 ℃

Note: The absolute maximum rating indicates the limit value that the device can withstand, exceeding the absolute maximum rating may cause permanent damage to the device. Working under absolute maximum rating conditions for long periods of time can affect the device Reliability of the device. Please pay attention to good heat dissipation under high temperature work.

Recommended Working Conditions

Parameters	Values
Drain voltage (V_{DD})	+28V (Typ)
Drain static current (I_{DQ})	350mA (Typ)
Gate voltage (V_{GG})	-2.3V (Typ)
Channel temperature (T_{CH})	225℃ (Max)
Storage temperature	-65℃ ~ +150℃
Operating temperature	-55℃ ~ +85℃

Note: Power amplifier tube electrical specifications are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

ESD Warnings

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

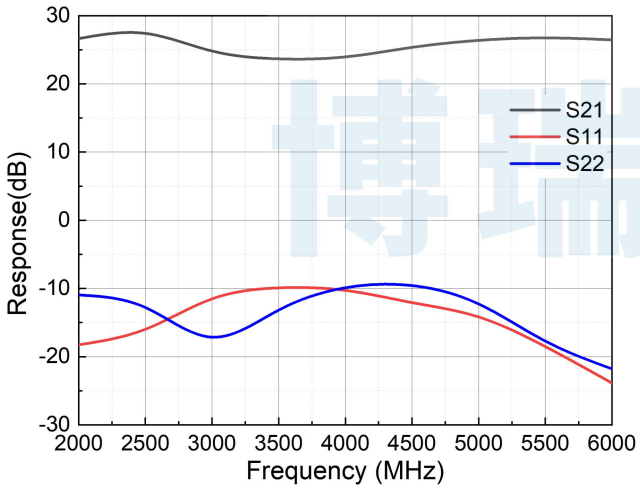
Typical Performance (EVB test data, 2GHz ~ 6GHz)

Parameters	Typ.									Units
Frequency	2000	2500	3000	3500	4000	4500	5000	5500	6000	MHz
Gain	26.65	27.41	24.83	23.68	23.95	25.35	26.37	26.74	26.45	dB
Small Signal Input Return	-18.26	-15.98	-11.52	-9.92	-10.28	-12.07	-14.18	-18.52	-23.87	dB
Small Signal Output Return	-10.96	-12.79	-17.13	-13.17	-9.9	-9.58	-12.27	-17.72	-21.78	dB
Drain Current @P_{sat}	0.961	1.137	1.188	1.137	1.267	1.354	1.228	1.085	0.997	A
Pout (dBm) @P_{sat}	41.26	41.89	41.56	40.97	41.26	41.72	41.8	41.3	41.17	dBm
PAE@P_{sat}	49.13	48.16	42.05	38.02	36.65	38.49	43.55	44.06	46.5	%
Power Gain @P_{sat}	19.63	21.09	16.32	14.97	15.63	17.46	19.68	21.1	20.67	dB
OIP3	46.4	47	44.9	44.3	44.7	45.4	47	46.9	46.8	dBm

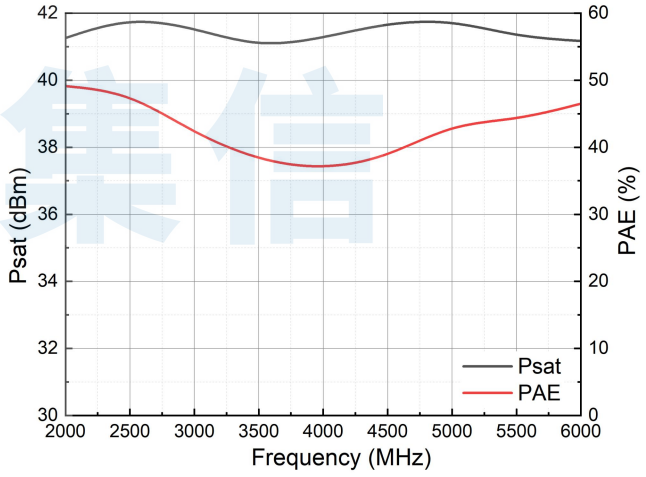
Test Conditions: Temp=+25℃CV_{DD}, =+28V, =I_{DQ}350mA, CW test, OIP3 Tone Spacing =1MHz, Pout per tone=34dBm;

Note: defined as the saturation power output by the evaluation board;P_{sat}

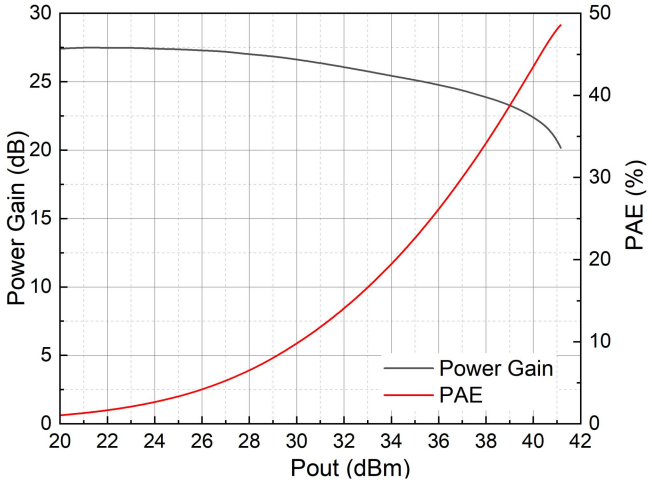
Typical Performance (EVB: 2GHz~6GHz, Temp =+25℃, V_{DD}=+28V, I_{DQ}=350mA, CW wave test)



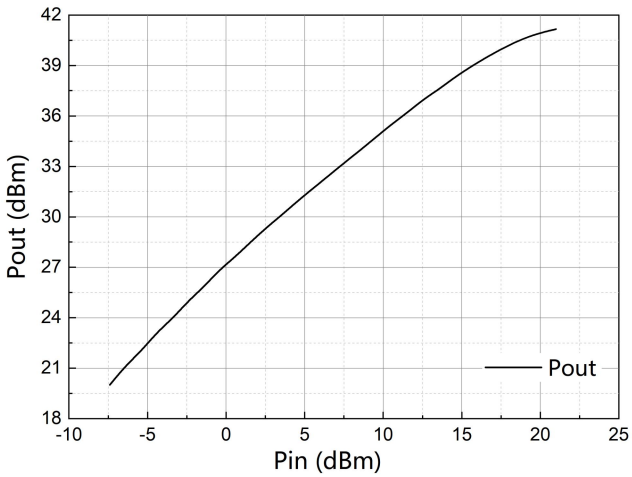
Gain,Output Return,Input Return vs. Freq



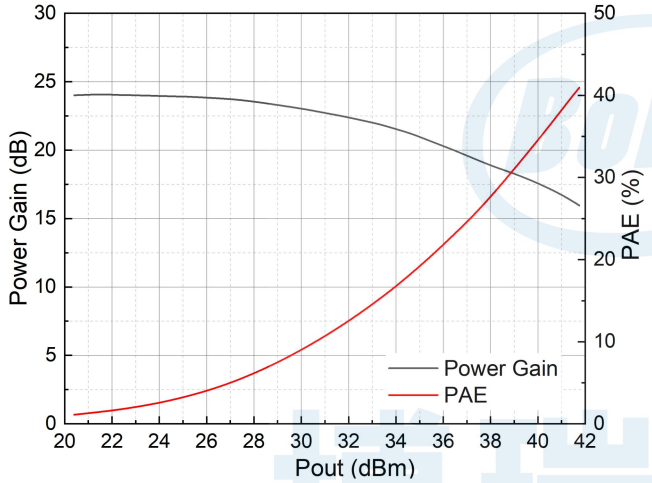
Saturated Output Power,Efficiency vs. Freq



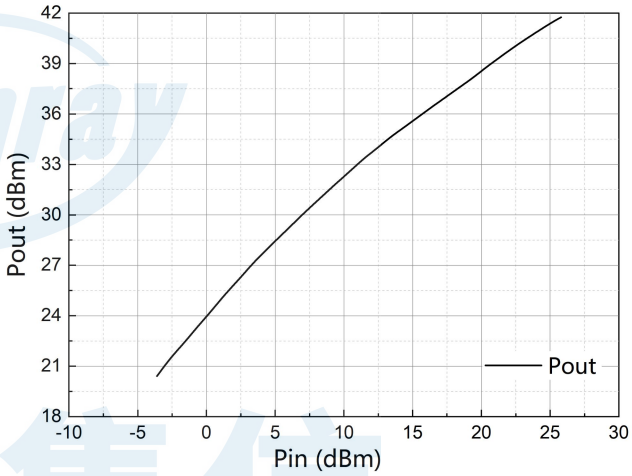
Gain,Efficiency vs. P_{out}@2GHz



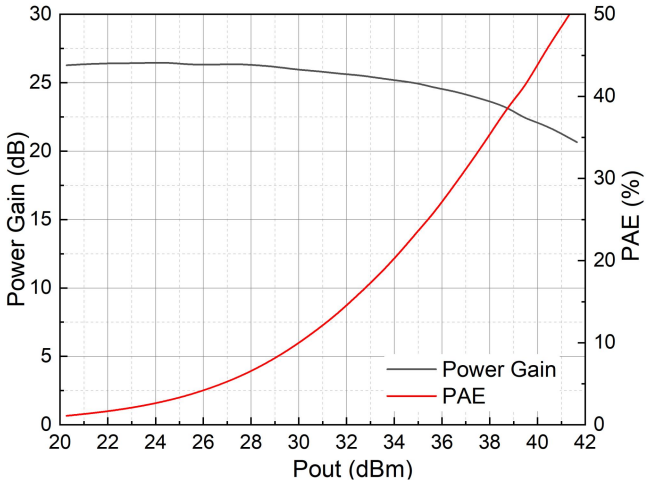
P_{out} vs. P_{in} @2GHz



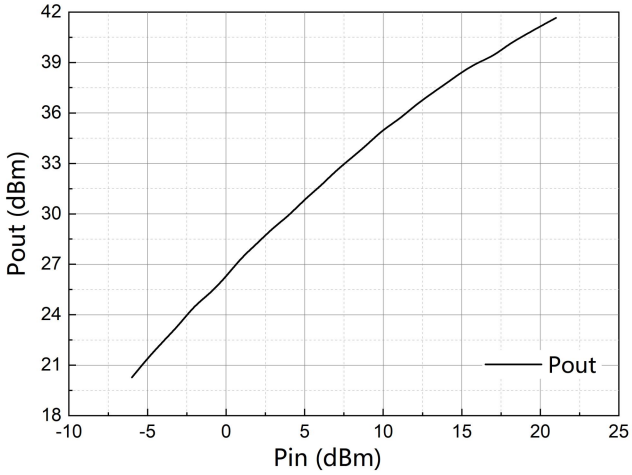
Gain,Efficiency vs. P_{out} @4GHz



P_{out} vs. P_{in} @4GHz

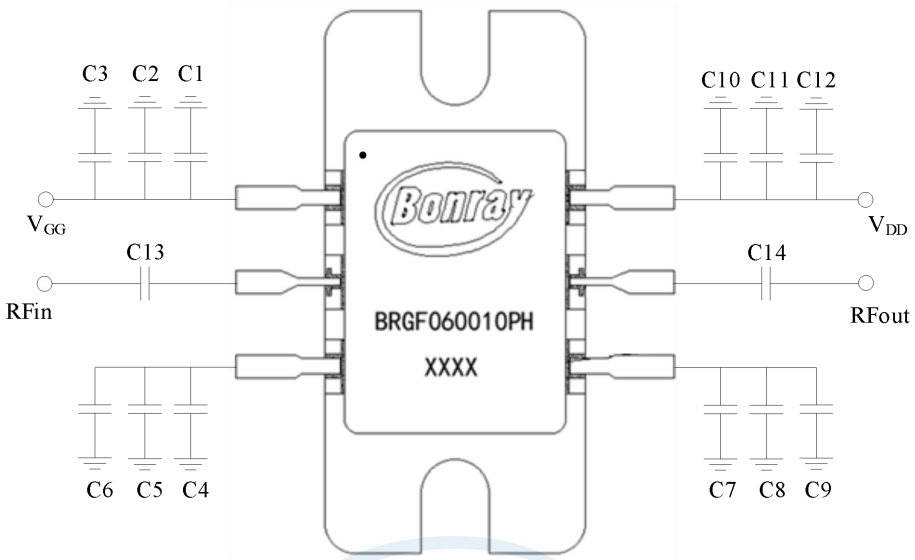


Gain,Efficiency vs. P_{out} @6GHz



P_{out} vs. P_{in} @6GHz

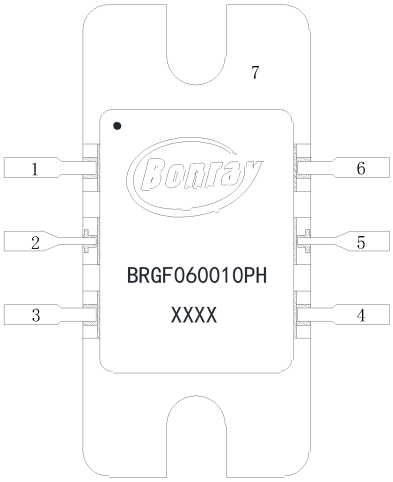
Typical Application Schematic



Bill of Material

Reference Designator	Package Size	Value	Model Number
C2,C3,C5,C6,C8,C9,C11,C12	1210	1210 10uF,100VDC	GRM32EC72A106KE05#
C1,C10	0603	1nF 50V ±10%	GCD188R71H102KA01D
C13,C14	0603	±5% 0Ω 1/10 W	RC0603JR-070RL
C4, C7	0603	51ohm,0603 package	RC0603FR-0751R1L

Pin Configuration and Description



Pin Number	Pin Name	Description
1	VGG	Amplifier gate, gate voltage regulation
2	RFin	Rf input
3, 4	NC	There is no internal electrical connection, and it is recommended to install it according to the recommended BOM
5	RFout	Rf signal output
6	VDD	Amplifier drain, drain voltage input
7	Metal housing	Amplifier source level, grounded, cooling

Power-on Sequence

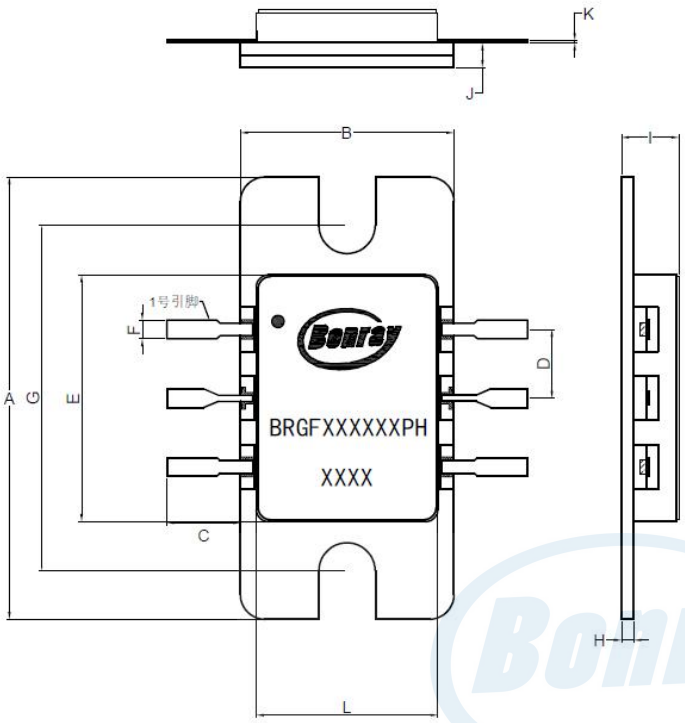
1. Set the gate voltage (V_{GG}) to -5V,
2. Set drain voltage (V_{DD}) to +28V, current limit 2A;
3. Open the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 350mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal;
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off the drain Supply Voltage voltage;
4. Turn off the gate Supply Voltage voltage;

Note: When the circuit is designed, the offset voltage needs to have a timing protection circuit to ensure that it is fully powered on before adding, and ensure that it is reduced to below 5V when powering off, before starting to power off; $V_{GG}V_{DD}V_{DD}V_{GG}$Especially in TDD Application, gate Supply Voltage decoupling capacitors need to be rigorously evaluated to meet switching speed requirements.

Package Dimensions (mm)



尺寸项	单位：mm		
	最小	中值	最大
A	17.83	18.03	18.23
B	8.55	8.7	8.85
C	2.5	3	3.5
D	2.67	2.8	2.93
E	9.9	10.05	10.2
F	0.63	0.76	0.9
G	13.88	14.08	14.28
H	0.37	0.5	0.63
I	2.25	2.4	2.55
J	0.8	1	1.2
K	0.07	0.1	0.13
L	7.25	7.4	7.55

Recommended Soldering Temperature Profile