Product Features

Frequency: 3.5GHz ~ 4.2GHz

Gain: 15.7dB@3.9GHz

Psat: 47.4dBm@3.9GHz

PAE: 51.7%@3.9GHz

V_{DD}Power Supply 28V, I_{DQ} 300mA

Package: PJ (metal package)

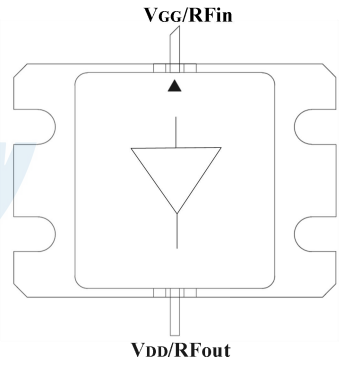
Package Factor

General Description

BRGF042050PJG is an internally matched power amplifier designed using the GaN HEMT process with 28V Supply.With high power additional efficiency; Thanks to the internal matching design, users can use only a small number of periphery components in the system.

BRGF042050PJG is housed in a metal ceramic shell package, with good reliability. The product is compact and easy to install, which is suitable for commercial and special communication application.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGF042050PJG	PJ	3.5 GHz to 4.2 GHz Internal Matched PA

Applications

Data Link

Radar

Universal Transmitter

Absolute Maximum Ratings

Parameters	Values
Gate drain breakdown voltage (BV_{DG})	100V
Gate pressure range (V_{GG})	-6 to 0V
Drain current (I_D)	6A
Gate current (I_G)	14mA
Continuous dissipated power (P_D)	75W
Continuous wave input power (P_{IN})	38dBm
Channel temperature (T_{CH})	275 ℃
Mounting temperature (30 seconds)	245 ℃

Note: The absolute maximum rating indicates the limit value that the device can withstand, exceeding the absolute maximum rating may cause permanent damage to the device. Working under absolute maximum rating conditions for a long period of time will affect the reliability of the device. Please pay attention to good heat dissipation under high temperature operation.

Recommended Working Conditions

Parameters	Values
Drain voltage (V_{DD})	+28V
Drain static current (I_{DQ})	300mA
Gate voltage (V_{GG})	2.4 V
Channel temperature (T_{CH})	225 ℃
Continuous dissipated power CW (P_D)	62W(25℃)
Storage temperature	-65℃ ~ +150℃
Operating temperature	-55℃ ~ +85℃

Note: The power amplifier tube electrical specifications are tested under the specified Test Condition. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	10:1

Test Condition: DEMO board test, =T_A25℃, V_{DD}=+28V, I_{DQ}=300mA, Freq=3.6GHz, CW wave, =40W P_{out}test;

Thermal Parameters

Parameters	Test Condition	Value	Units
Thermal resistance (θ_{JC})	DC at 85 ° C case	3.3	℃/W

Note: θ_{JC} to measure the thermal resistance to the bottom of the tube housing;

ESD Warnings

ELECTROSTATIC SENSITIVE DEVICE

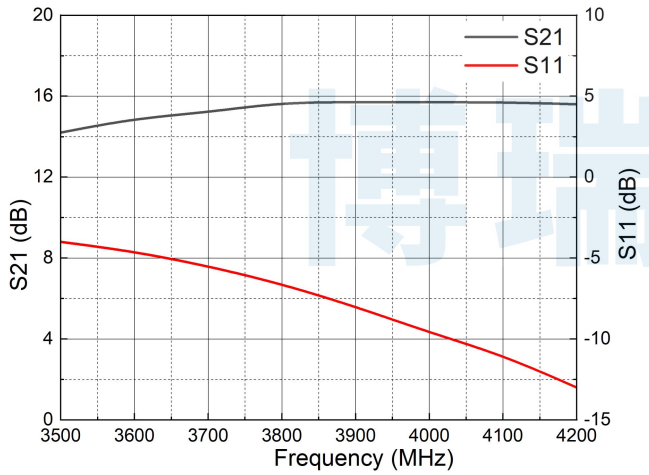
OBSERVE HANDLING PRECAUTIONS

RF Features :EVB Test Data (3.5GHz ~ 4.2GHz)

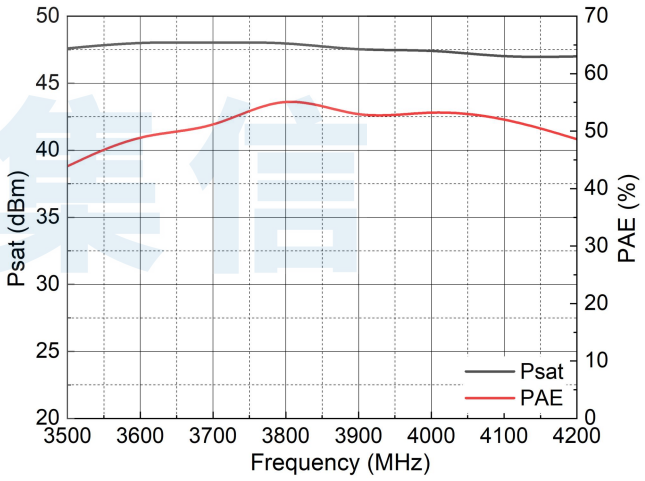
Parameters	Typ.								Units
Frequency	3500	3600	3700	3800	3900	4000	4100	4200	MHz
Gain	14.2	14.9	15.2	15.7	15.7	15.7	15.7	15.6	dB
Small Signal Input Return	-4.0	-4.6	-5.5	-6.6	-8.0	-9.6	-11.0	-13.0	dB
Drain Current @P_{sat}	4.20	4.14	4.14	3.78	3.55	3.55	3.11	3.47	A
Pout (dBm) @P_{sat}	47.6	48.1	48	48.1	47.4	47.55	46.9	47	dBm
Power Gain @P_{sat}	9.9	9.8	10.9	12.1	11.9	12.25	11.8	12.3	dB
PAE@P_{sat}	43.9	49.8	50.0	57.2	51.7	53.8	52.4	48.6	%
Test Condition: Temp =+25℃CV_{DD}, =+28V, =300mA, CW test									

Note: Defined as the saturation power output of the evaluation board P_{sat}.

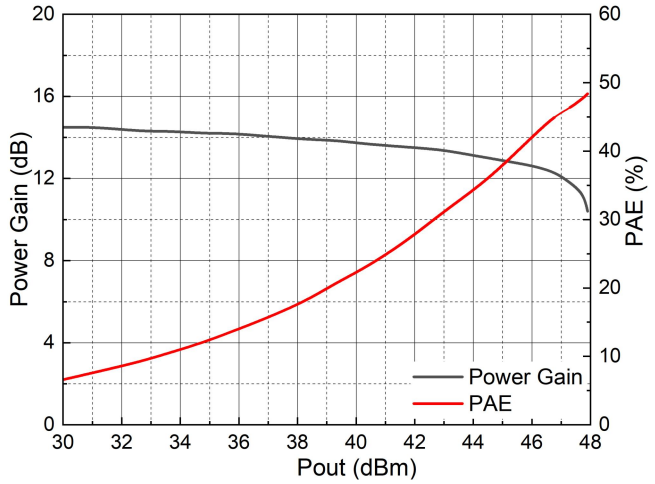
Typical Performance (Evaluation board: 3.5GHz~4.2GHz, Temp=+25℃, V_{DD}=+28V, I_{DQ}=300mA, CW wave test)



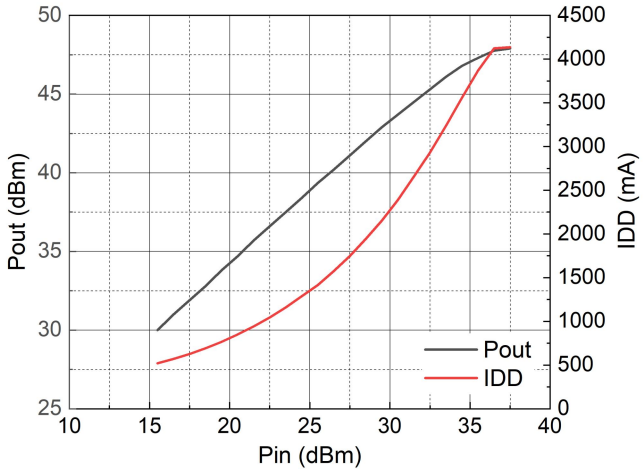
Gain, Input Return vs. Freq



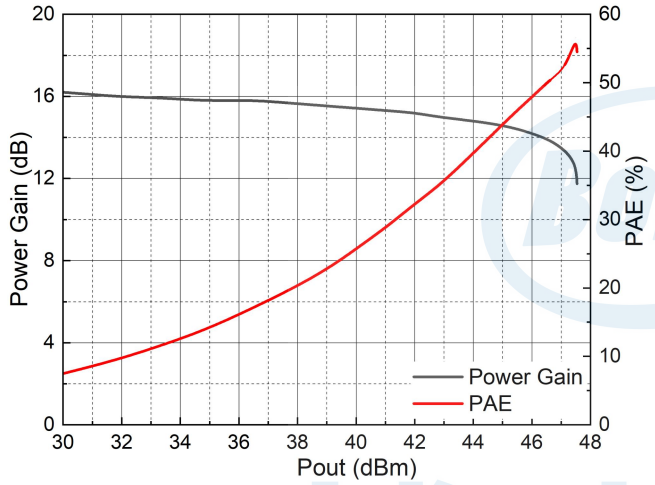
Saturated Power, Efficiency vs. Freq



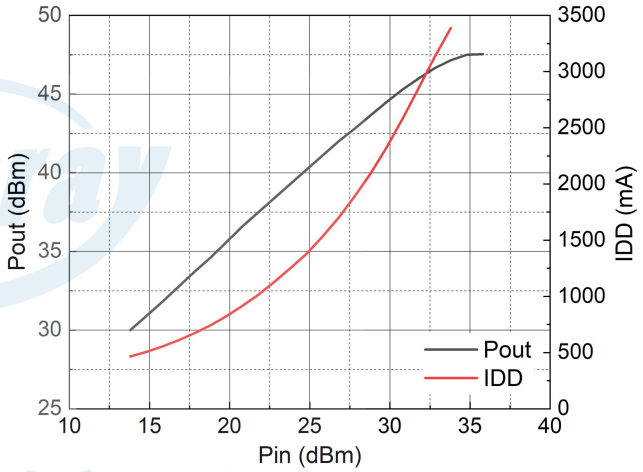
Gain, Efficiency vs. P_{out} @3.7GHz



P_{out} , IDD vs. Input Power @3.7GHz

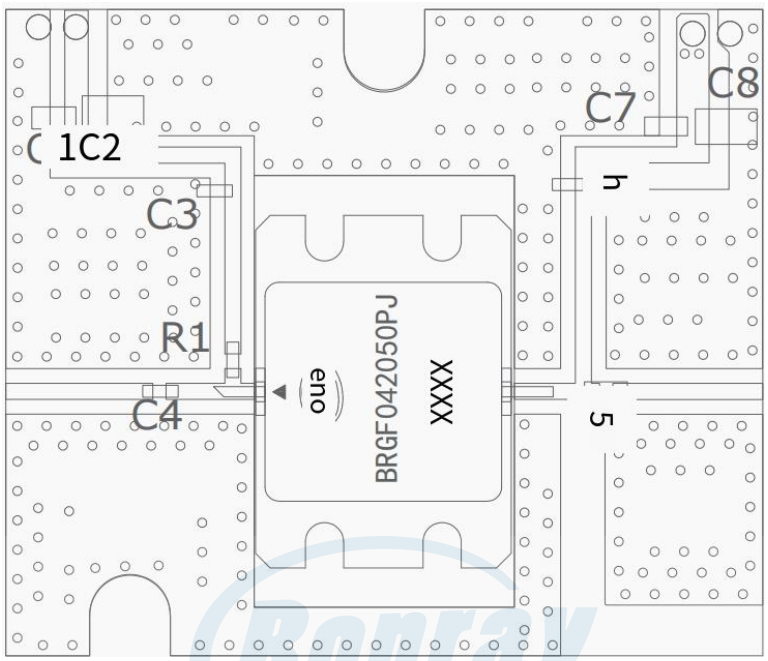


Gain, Efficiency vs. P_{out} @4GHz

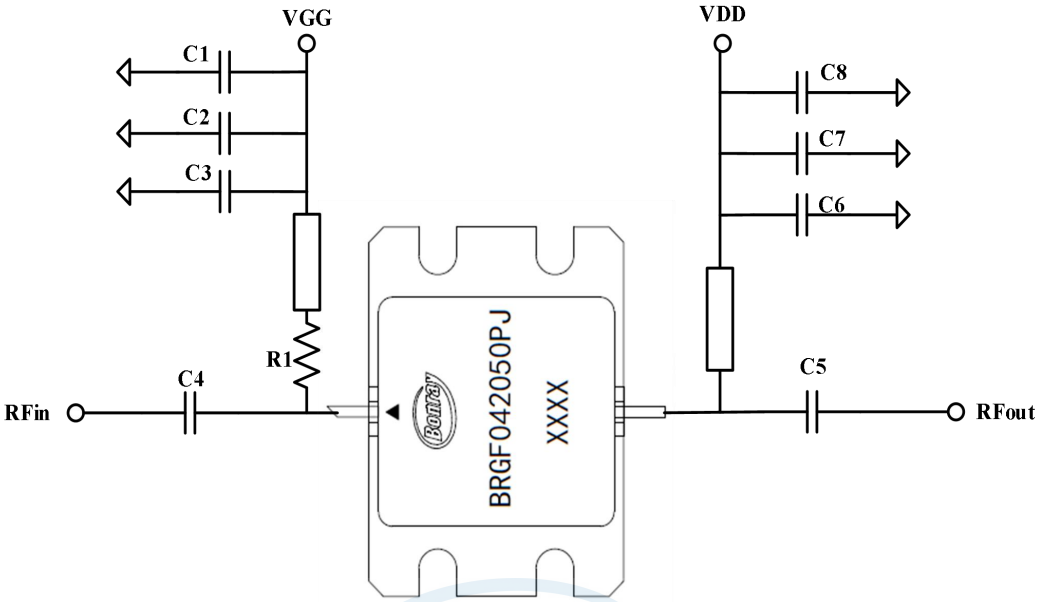


P_{out} , IDD vs. Input Power @4GHz

Assembly Diagram



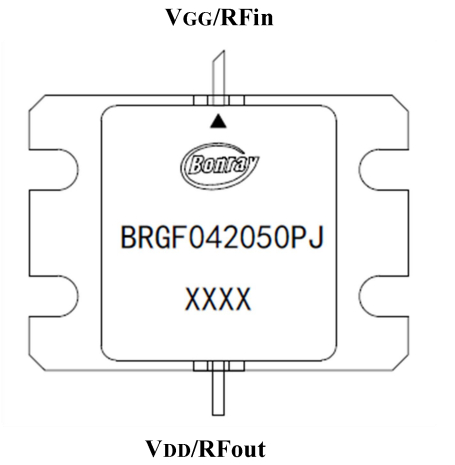
Typical Application Schematic



Bill of Material

Reference Designator	Packaging	Value	P/N
C3,C4,C5,C6	0603	2.4 pF	GQM1875C2E2R4BB12#
C2,C8	1210	10uF	GRM32EC72A106KE05#
C1	1206	0.1 uF	GRM31C5C2A104JA01#
R1	0805	30ohm	CRT0805-FX-30R0ELF
C7	0805	39pF	VJ0805D390JXPQJHT
C9	/	0.2 pF	600L0R2BT200T

Pin Configuration and Description



Pin Number	Pin Name	Description
1	V_{GG}/RFin	Gate, gate voltage regulation, RF signal 50Ω system input
2	V_{DD}/RFout	Drain, drain voltage input, RF power signal 50Ω system output
-	Package Base	Device housing, to be welded or well coated on the bottom Mount to the heat dissipation and ground network substrate to ensure good heat dissipation and RF grounding

Power-on Sequence

1.Steps 1 Set the gate voltage (V_{GG}) to -5V

2. Set drain voltage (V_{DD}) to +28V with current limit 6A

3 Turn on the gate voltage

4. Turn on drain voltage

5 Increase the gate voltage (V_{GG}) so that the drain current is 300mA

6. Input the RF signal

Power-off Sequence

1. Turn off the RF signal

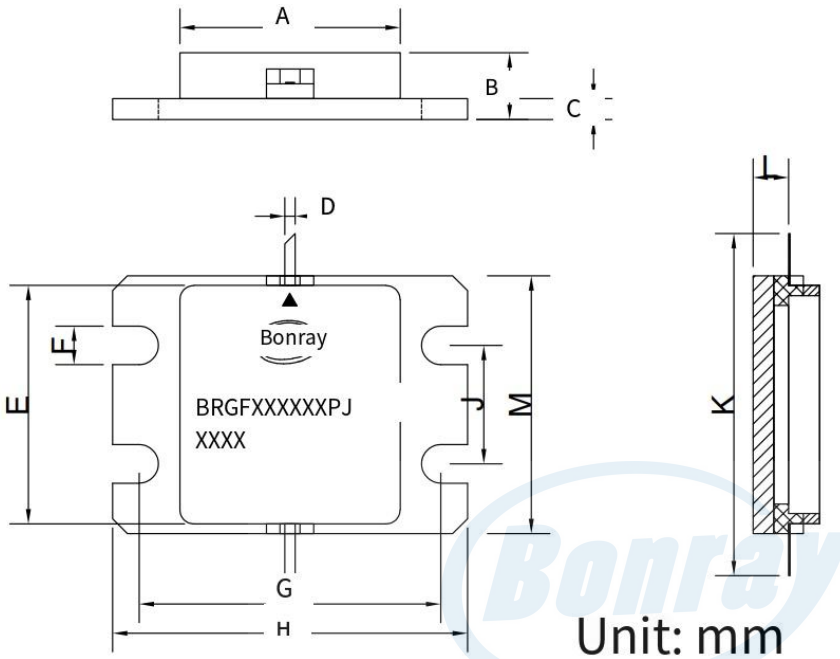
2. Reduce the gate voltage (V_{GG}) to -5V

3. Turn off drain supply voltage

4. Turn off the gate supply voltage

Note: When the circuit is designed, the offset voltage needs to have a timing protection circuit to ensure that it is fully powered on before adding, and ensure that it is reduced to below 5V when powering off, before starting to power off; $V_{GG}V_{DD}V_{DD}V_{GG}$Especially in TDD applications, gate supply decoupling capacitors need to be rigorously evaluated to meet the switching speed requirements.

Package Dimensions (mm)



DIM	MILIMETER MIN.	MILIMETER MAX.	DIM	MILIMETER MIN.	MILIMETER MAX.
A	14.77	15.03	G	20.27	20.53
B	4.3	47	H	23.85	24.15
C	1.27	1.53		17.55	7.87	8.13
D	0.6	0.8	K	26.2	26.8
E	15.97	16.23	L	2.25	2.55
F	2.6		M	17.25	

Recommended Soldering Temperature Profile