Product Features

Frequency: 2.7GHz ~ 3.5GHz

Gain: 15.9dB@3.1GHz

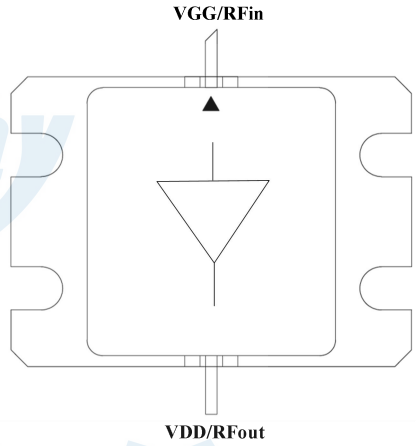
Psat: 47.9dBm@3.1GHz

PAE: 52.9%@3.1GHz

V_{DD}Power Supply 28V, static current 300mA

Package: PJ (metal package)

Functional Block Diagram



General Description

BRGF035050PJG is an internally matched power amplifier designed using the GaN HEMT process with 28V Supply. Thanks to the internal matching design, users can use only a small number of periphery components in the system. In addition, the product is compact, easy to install, suitable for commercial and special communication.

Application

Power Amplification Stage for Wireless Infrastructure

Test and Measurement Equipment

Universal Transmitters and Jammers

Ordering Information

Part Number	Package	Description
BRGF035050PJG	PJ	2.7 GHz to 3.5 GHz Internal Matched PA

Absolute Maximum Ratings

Parameters	Values
Gate drain breakdown voltage (BV_{DG})	100V
Gate pressure range (V_{GG})	-6 to 0V
Drain current (I_D)	6A
Gate current (I_G)	14mA
Continuous dissipated power (P_D)	80W
Continuous wave Pin (dBm) (P_{IN})	37dBm
Channel temperature (T_{CH})	275 ℃
Mounting temperature (30 seconds)	245 ℃

Note: The absolute maximum rating indicates the limit value that the device can withstand, exceeding the absolute maximum rating may cause permanent damage to the device. Working under absolute maximum rating conditions for a long period of time will affect the reliability of the device. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Values
Drain voltage (V_{DD})	+28V
Drain static current (I_{DQ})	300mA
Gate voltage (V_{GG})	2.4 V
Channel temperature (T_{CH})	225 ℃
Continuous dissipated power CW (P_D)	62W(25℃)
Storage temperature	-65℃ ~ +150℃
Operating temperature	-55℃ ~ +85℃

Note: The electrical specifications of the amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when operating outside of the test specifications.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test Conditions: DEMO board test, $=T_A$25℃, V_{DD}=+28V,I_{DQ}=300mA, Fre=2GHz, CW wave, =50W P_{out}test;

Thermal Parameters

Parameters	Test Conditions	Value	Units
Thermal resistance (θ_{JC})	DC at 85 ° C case	3.3	℃/W

Note: θ_{JC} to measure the thermal resistance to the bottom of the tube housing;

ESD Warnings

ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

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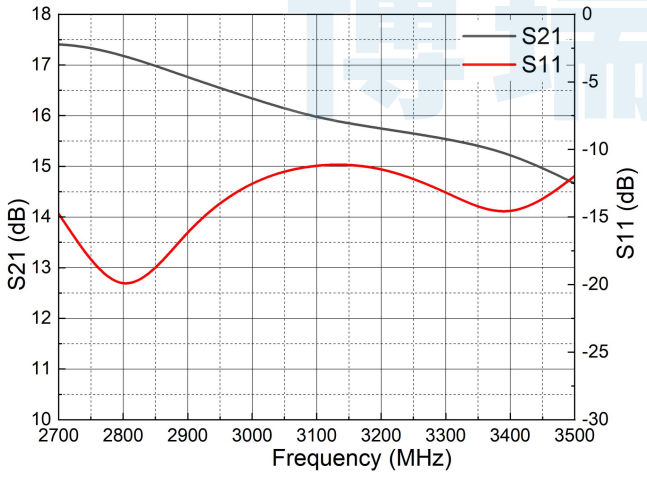
RF Features, Evaluation Board Test Data (2.7GHz ~ 3.5GHz)

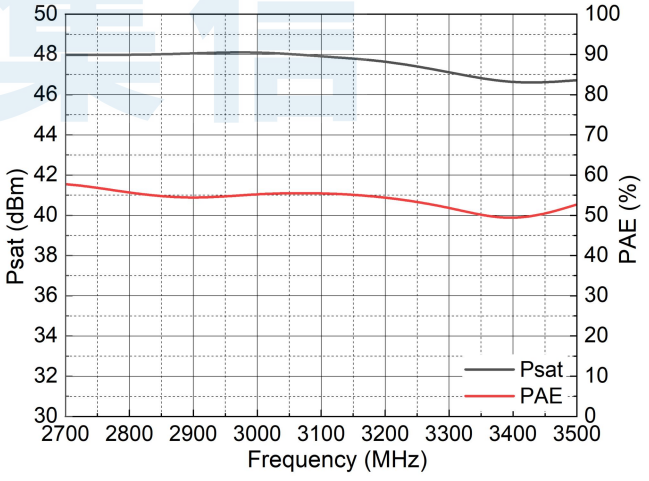
Specifications	Typ.									Units
Frequency	2700	2800	2900	3000	3100	3200	3300	3400	3500	MHz
Gain	17.5	17.2	16.8	16.3	15.9	15.7	15.6	15.3	14.7	dB
Small Signal Input Return	-14.5	-22.3	-15.6	-12.2	-11.0	-11.2	-13.1	-15.6	-12.0	dB
Drain Current @P_{sat}	3.62	3.76	3.90	3.89	3.70	3.58	3.28	3.08	2.91	A
Output Power @P_{sat}	48.0	48.0	48.1	48.2	47.9	47.7	47.1	46.5	46.7	dBm
Power Gain @P_{sat}	12.0	11.9	11.1	11.2	11.8	11.5	11.4	11.4	10.6	dB
PAE@P_{sat}	58.3	55.5	53.9	55.4	55.7	54.7	52.1	47.9	52.7	%
Test Conditions: Temp =+25℃V_{DD}, =+28V, =I_{DQ}300mA, CW test;										

Note: defined as the saturation power output by the evaluation board;P_{sat}

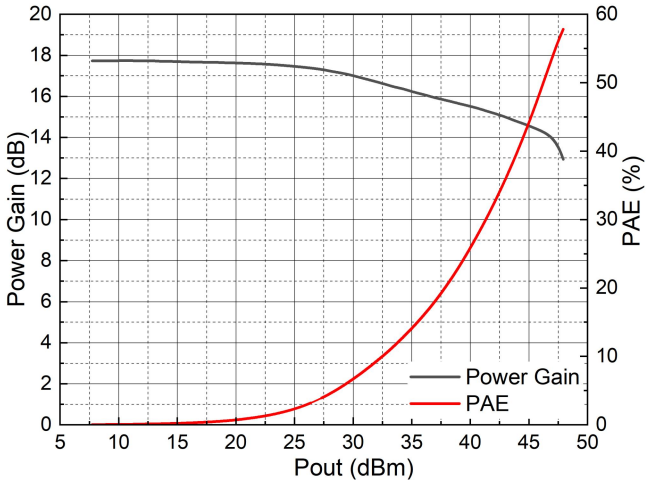
Typical Performance (Evaluation board :2.7GHz ~ 3.5GHz, Temp =+25℃, V_{DD}=+28V, I_{DQ}=300mA, CW wave test)



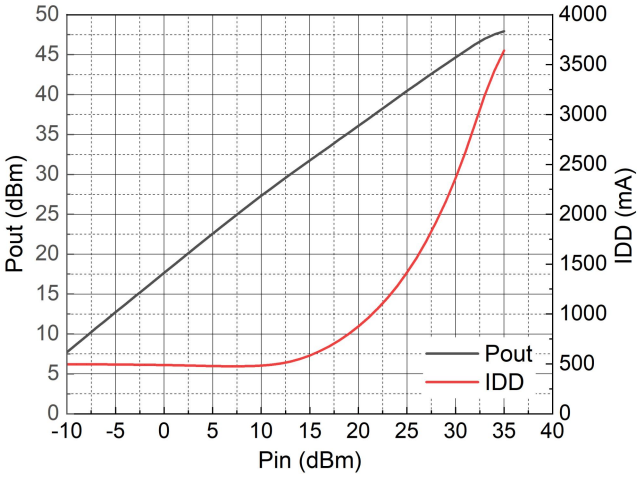
Gain, Input Return vs. Freq



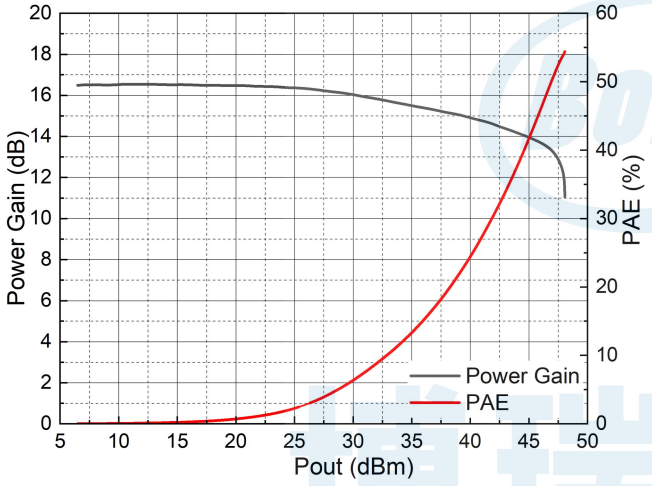
Saturated Power, Efficiency vs. Freq



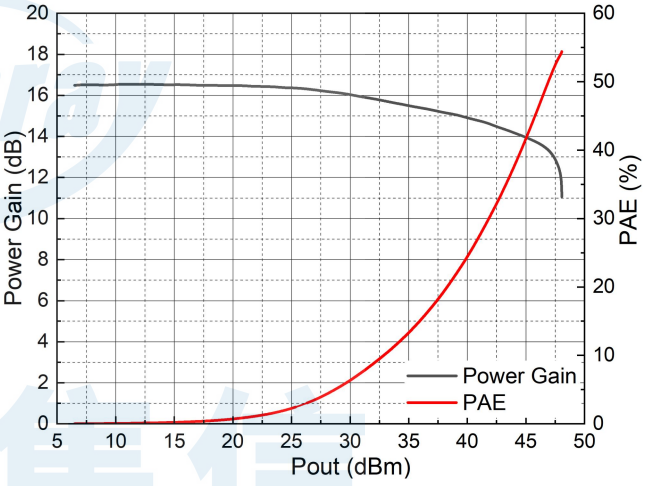
Gain, Efficiency vs. P_{out} @2.7GHz



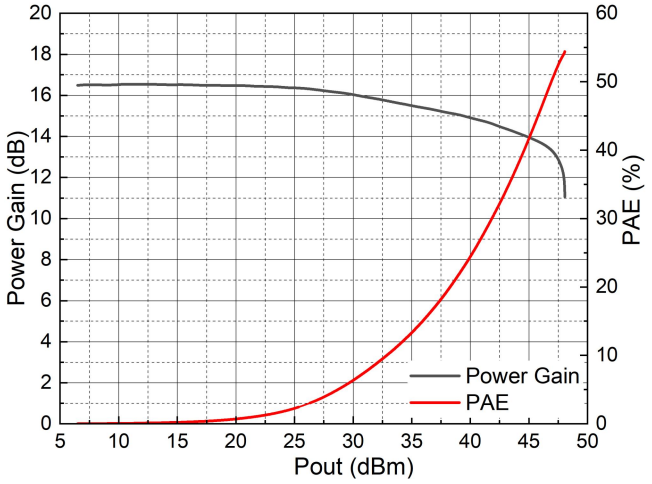
P_{out} vs. Pin @2.7GHz



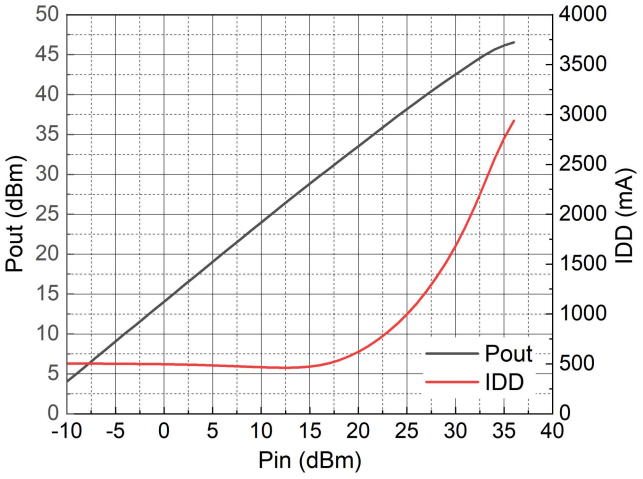
Gain, Eficiency vs. P_{out} @3GHz



P_{out} vs. Pin @13GHz

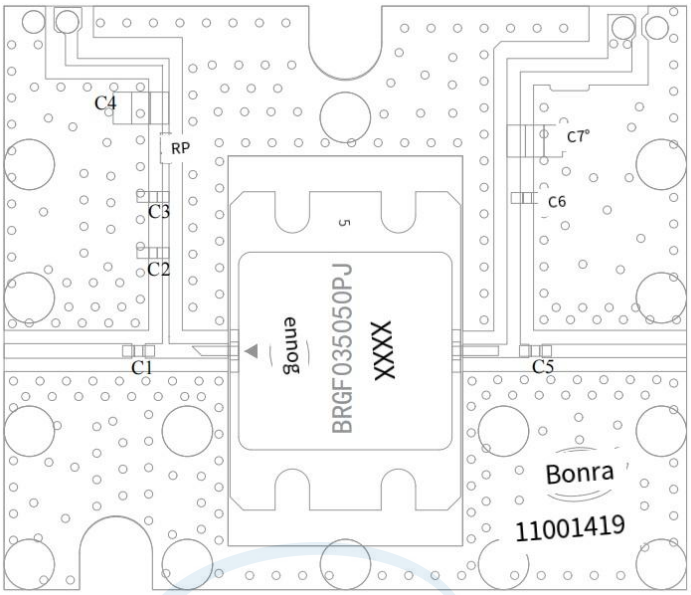


Gain, Efficiency vs. $P_{out@}$3.5GHz

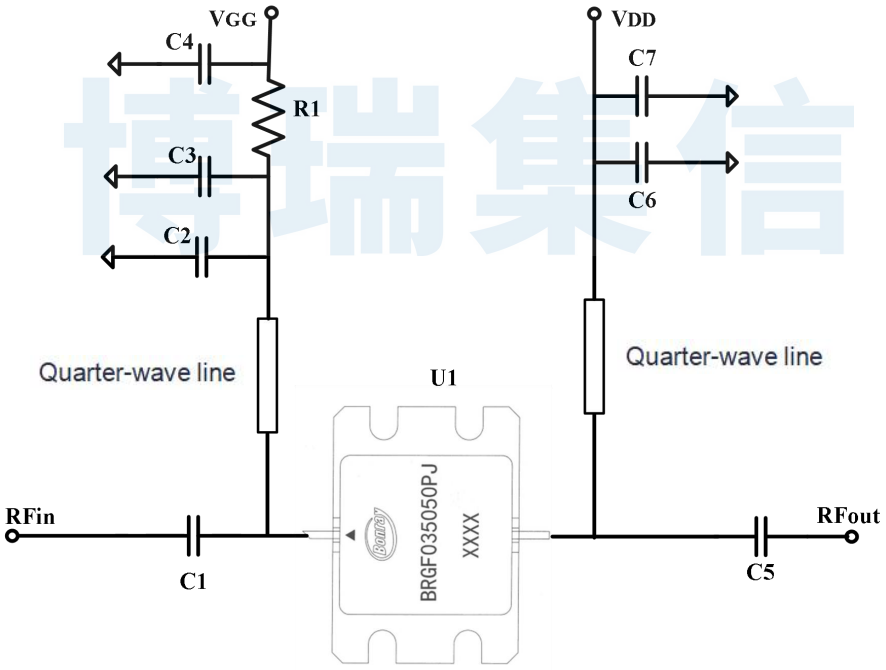


P_{out} vs. Pin @3.5GHz

PCB Evaluation Board



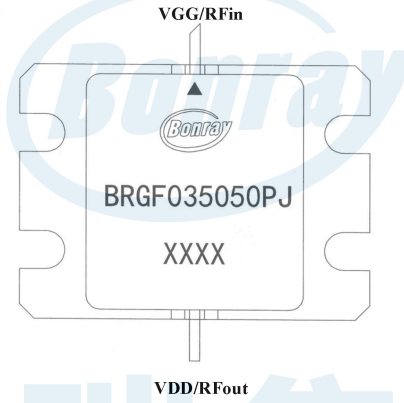
Typical Application Schematic



Bill of Material

Designator	Packaging	Value	Part Number
U1	PJ	50W	BRGF035050PJ
C1,C5,C6	0603	6.8 pF	GQM1875G2E6R8BB12#
C2	0603	33pF	GQM1875C2E330FB12#
C3	0603	200pF	0603B201K500NT
C4,C7	1210	10uF,100VDC	GRM32EC72A106KE05#
R1	0603	30ohm	RC0603FR-0730RL

Pin Configuration and Description



Pin Number	Pin Name	Description
1	VGG/RFin	Gate, gate voltage regulation, RF signal 50Ω system input
2	VDD/RFout	Drain, drain voltage input, RF power signal 50Ω system output
-	Package Base	The shell must be welded or coated at the bottom. The shell must be installed on the heat dissipation and ground network substrate to ensure good heat dissipation and RF grounding

Power-on Sequence

1. Set the gate voltage (V_{GG}) to -5V;
2. Set drain voltage (V_{DD}) to +28V, current limit 6A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 300mA;

Power-off Sequence

1. Turn off the RF signal;
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off drain supply voltage;
4. Turn off the gate supply voltage;

Note: When the circuit is designed, the offset voltage needs to have a timing protection circuit to ensure that it is fully powered on before adding, and ensure that it is reduced to below 5V when powering off, before starting to power off; $\mathbf{V_{GG}V_{DD}V_{DD}V_{GG}}$ Especially in TDD Application, gate-supplied decoupling capacitors need to be rigorously evaluated to meet switching speed requirements.

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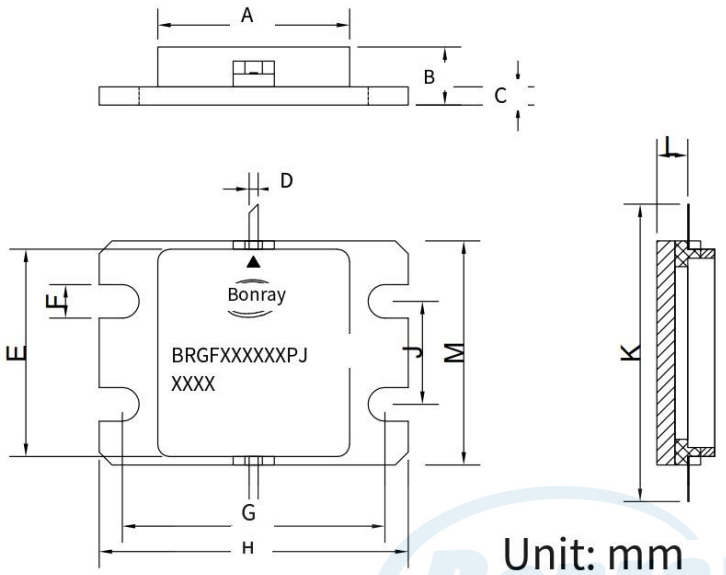
Package Dimensions (mm)

PJ package



DIM	MILIMETER MIN.	MILIMETER MAX.	DIM	MILIMETER MIN.	MILIMETER MAX.
A	14.77	15.03	G	20.27	20.53
B	4.3	47	H	23.85	24.15
C	1.27	1.53		7.87	8.13
D	0.6	0.8	K	26.2	26.8
E	15.97	16.23	L	2.25	2.55
F	2.6		M	17.25	

Unit: mm

Recommended Soldering Temperature Profile