Product Features

Frequency: 2.0GHz ~ 2.4GHz

Gain: 18.6dB@2.2GHz

Psat: 47.8dBm@2.2GHz

PAE: 62.9%@2.2GHz

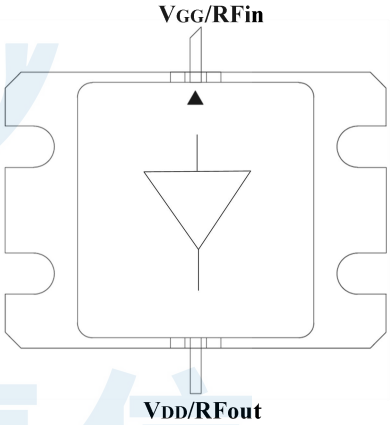
V_{DD}Supply Voltage 28V, I_{DQ} 300mA

Package: PJ (metal package)

General Description

The BRGF024050PJG is an internally matched power amplifier fabricated by GaN HEMT process. The product adopts 28V Supply Voltage at the drain and has high power added efficiency. Thanks to the internal matching design, users can use only a small number of periphery components in the system, the product is packaged with metal ceramic shell, with good reliability. Compact and easy to install for commercial and special communication application.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGF024050PJG	PJ	2.0 GHz to 2.4 GHz Internal Matched PA

Application

Power Amplification Stage for Wireless Infrastructure

Test and Measurement Equipment

Universal Transmitters and Jammers

Absolute Maximum Ratings

Parameters	Values
Gate drain breakdown voltage (BV_{DG})	100V
Gate pressure range (V_{GG})	-6 to 0V
Drain current (I_D)	6A
Gate current (I_G)	14mA
Continuous dissipated power (P_D)	75W
Continuous wave input power (P_{IN})	35dBm
Channel temperature (T_{CH})	275 ℃
Mounting temperature (30 seconds)	245 ℃

Note: The absolute maximum rating indicates the limit value that the device can withstand, exceeding the absolute maximum rating may cause permanent damage to the device. Working under absolute maximum rating conditions for a long period of time will affect the reliability of the device. Please pay attention to good heat dissipation under high temperature operation.

Recommended Working Conditions

Parameters	Values
Drain voltage (V_{DD})	+28V
Drain static current (I_{DQ})	300mA
Gate voltage (V_{GG})	2.4 V
Channel temperature (T_{CH})	225 ℃
Continuous dissipated power CW (P_D)	62W(25℃)
Storage temperature	-65℃ ~ +150℃
Operating temperature	-55℃ ~ +85℃

Note: Power amplifier tube electrical specifications are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test conditions: DEMO board test, = T_A 25℃, V_{DD}=+28V, I_{DQ}=300mA, Freq=2GHz, CW wave, =50W P_{out}test;

Thermal parameters

Parameters	Test Conditions	Value	Units
Thermal resistance (θ_{JC})	DC bias tested at 85 ° C case	3.3	℃/W

Note: θ_{JC} to measure the thermal resistance to the bottom of the tube housing;

ESD Warnings

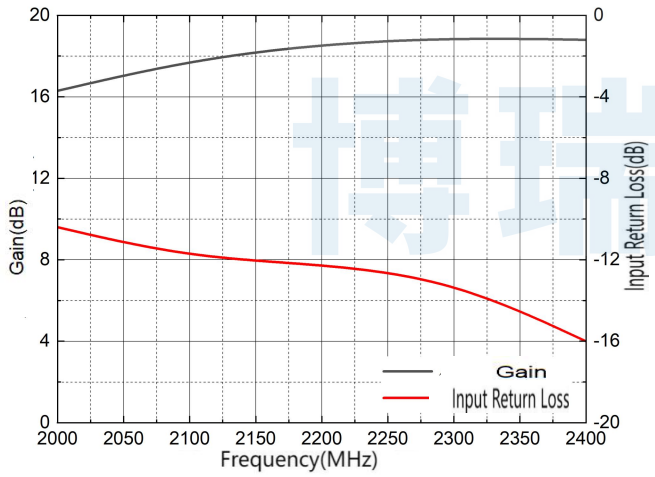
ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

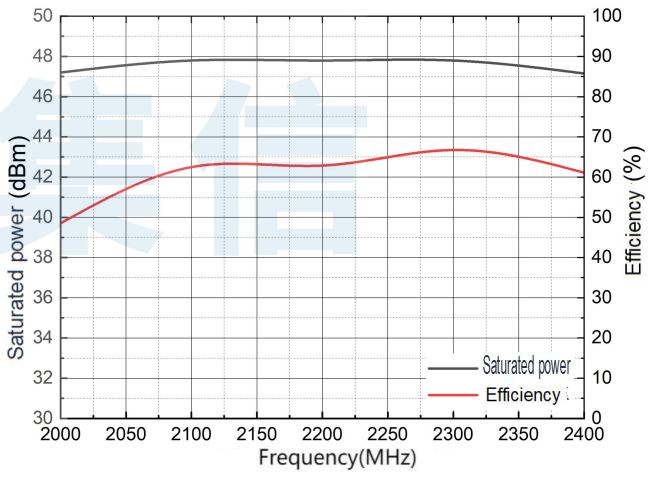
RF Features: Evaluation Board (2.0GHz ~ 2.4GHz) Test Data

Parameters	Typ.					Units
Frequency	2000	2100	2200	2300	2400	MHz
Gain	16.3	17.8	18.6	18.9	18.8	dB
Small Signal Input Return	-10.4	-11.9	-12.2	-13.0	-16.0	dB
Drain Current @P_{sat}	3.65	3.30	3.30	3.10	2.92	A
Output Power @P_{sat}	47.20	47.80	47.80	47.80	47.20	dBm
Power Gain @P_{sat}	13.0	15.0	15.0	14.8	14.5	dB
PAE@P_{sat}	48.53	62.49	62.86	66.73	61.09	%
Test Conditions: Temp =+25℃V_{DD}, =+28V, =I_{DQ}300mA, CW test; Note: defined as the saturation P_{sat}power output by the evaluation board;						

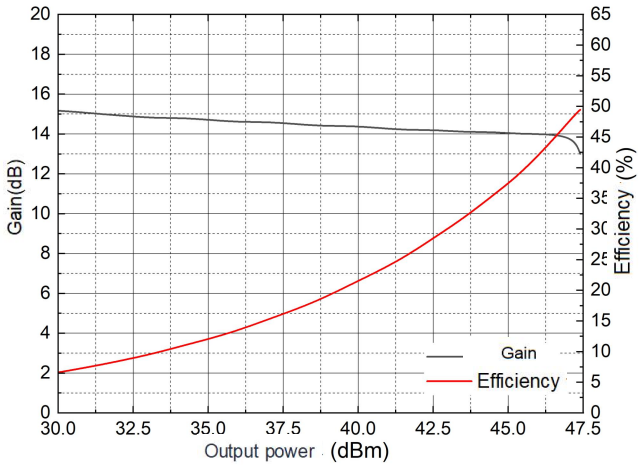
Typical Performance (Evaluation board: 2.0GHz~2.4GHz, Temp=+25℃, V_{DD}=+28V, I_{DQ}=300mA, CW wave test)



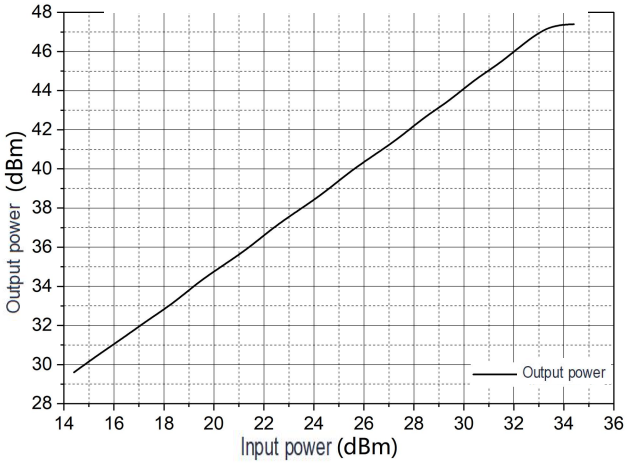
Input Return, Gain vs Freq



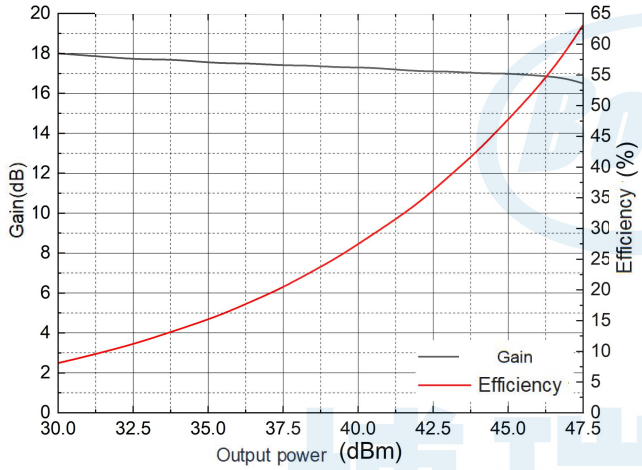
Saturation power, Efficiency vs Freq



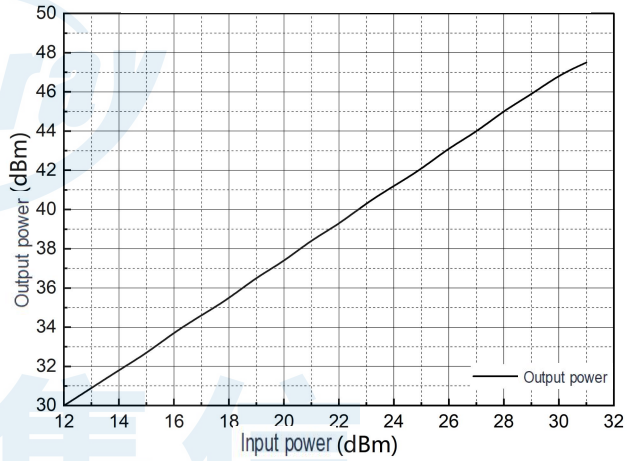
Gain, Efficiency, vs P_{out}@2GHz



P_{out} vs pin@2GHz

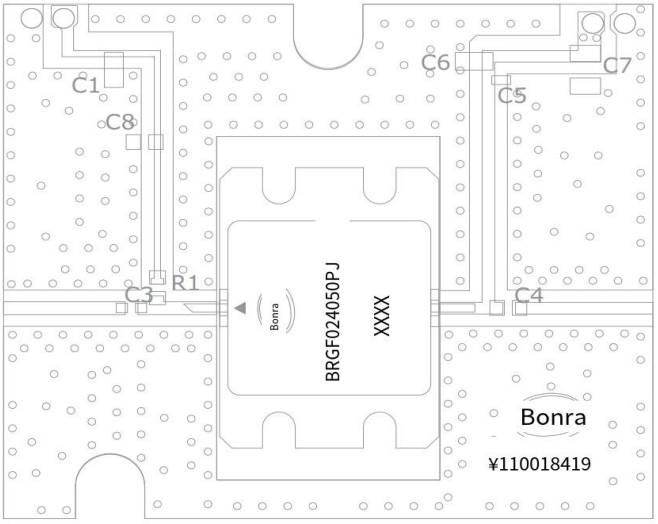


Gain, Efficiency, vs P_{out}@2.3 GHz

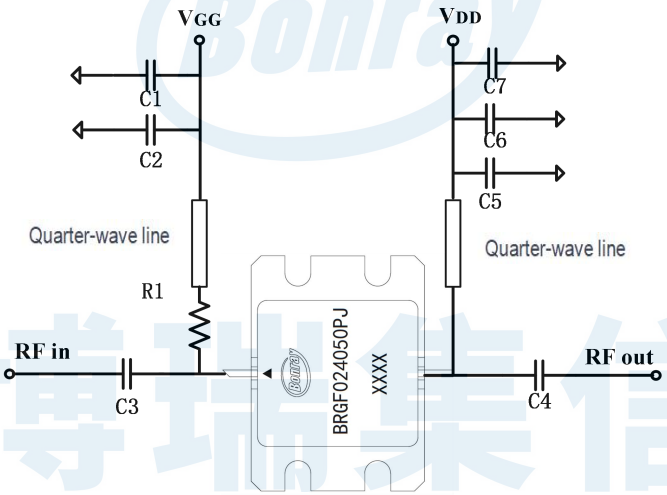


P_{out} vs pin@2.3GHz

Typical Application Schematic



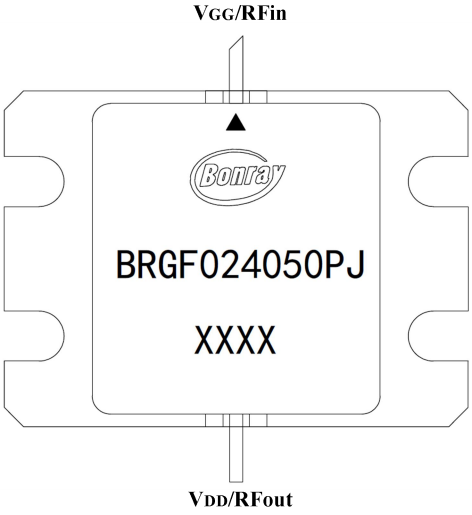
Assembly Diagram



Bill of Material

Reference Designato	Package Size	Value	Part Number
C5,C3	0603	33pF	GQM1875C2E330FB12#
R1	0805	30ohm	CRT0805-FX-30R0ELF
C4	0805	100pF	VJ0805D101JXPAJ
C8	0805	39pF	VJ0805D390JXPQJHT
C1,C6	1206	4.7 uF	GRM31CC72A475KE11#
C7	1210	10uF	GRM32EC72A106KE05#

Pin Configuration and Description



Pin Number	Pin Name	Description
1	V_{GG}/RFin	Gate, gate voltage regulation, RF signal 50Ω system input
2	V_{DD}/RFout	Drain, drain voltage input, RF power signal 50Ω system output
-	Package Base	Device housing, to be welded or well coated on the bottom Mount to the heat dissipation and ground network substrate to ensure good heat dissipation and RF grounding

Power-on Sequence

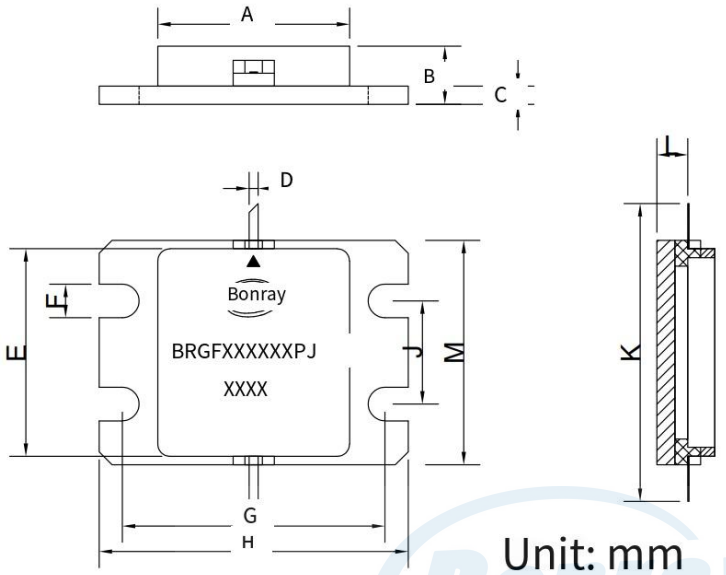
1. Set the gate voltage (V_{GG}) to -5V;
2. Set drain voltage (V_{DD}) to +28V, current limit 6A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}), so that the drain current is 300mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal.
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off the drain Supply Voltage voltage;
4. Turn off the gate Supply Voltage voltage;

Note: When the circuit is designed, the bias voltage needs to have a timing protection circuit to ensure that it is fully powered on and then added, and ensure that it is reduced to below 5V when powered off before starting to power off; $V_{GG}V_{DD}V_{DD}V_{GG}$Especially in TDD Application, gate Supply Voltage decoupling capacitors need to be rigorously evaluated to meet switching speed requirements.

Package Dimensions (mm)



DIM	MILIMETER		DIM	MILIMETER	
	MIN.	MAX		MIN.	MAX
A	14.77	15.03	G	20.27	20.53
B	4.3	4.7	H	23.85	24.15
C	1.27	1.53	J	7.87	8.13
D	0.6	0.8	K	26.2	26.8
E	15.97	16.23	L	225	2.55
F	2.6		M	17.25	17.55

Unit: mm

Recommended Soldering Temperature Profile