Product Features

Frequency: 1.9GHz ~ 2.2GHz

Gain: 16.1dB@2GHz

Saturated Pout (dBm): 48dBm@2GHz

PAE: 61.5%@2GHz

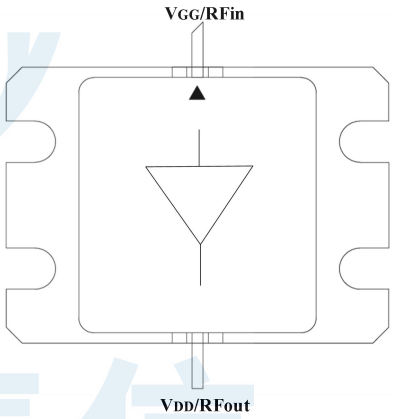
V_{DD}Power Supply 28V, I_{DQ} 300mA

Package: PJ (metal package)

General Description

BRGF021050PJG is is an internally matched power amplifier designed using the GaN HEMT process with 28V power supply. The power added efficiency is high. And thanks to the internal matching design, users can apply it to the system design with only a few external devices. The product adopts metal ceramic shell package, which has good reliability. The product is compact and easy to install, suitable for commercial and special communication applications.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGF021050PJG	PJ	1.9 GHz to 2.2 GHz Internal Matched PA

Applications

Power Amplification Stage for Wireless Infrastructure

Test and Measurement Equipment

Universal Transmitters and Jammers

Absolute Maximum Ratings

Parameters	Values
Gate drain breakdown voltage (BV_{DG})	100V
Gate pressure range (V_{GG})	-6 to 0V
Drain current (I_D)	6A
Gate current (I_G)	14mA
Continuous dissipated power (P_D)	75W
Continuous wave input power (P_{IN})	37dBm
Channel temperature (T_{CH})	275 ℃
Mounting temperature (30 seconds)	245 ℃
Storage temperature	-65℃ ~ +150℃
Operating temperature	-55℃ ~ +85℃

Note: The absolute maximum rating indicates the limit value that the device can withstand, exceeding the absolute maximum rating may cause permanent damage to the device. Working under absolute maximum rating conditions for a long period of time will affect the reliability of the device. Please pay attention to good heat dissipation under high temperature operation.

Recommended Working Conditions

Parameters	Values
Drain voltage (V_{DD})	+28V
Drain static current (I_{DQ})	300mA
Gate voltage (V_{GG})	2.4 V
Channel temperature (T_{CH})	225 ℃
Continuous dissipated power CW (P_D)	62W (25 ° C)

Note: Power amplifier tube electrical specifications are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Symbol	Parameters	Typ.
VSWR	Impedance mismatch Ruggedness	5:1

Test Conditions: DEMO board test, $=T_A$25℃, V_{DD}=+28V, I_{DQ}=300mA, Freq=2GHz, CW wave, =50W P_{out}test;

Thermal Parameters

Parameters	Test Conditions	Value	Units
Thermal resistance (θ_{JC})	Dc bias tested at 85 ° C	3.3	℃/W

Note: θ_{JC} to measure the thermal resistance to the bottom of the tube housing;

ESD Warnings

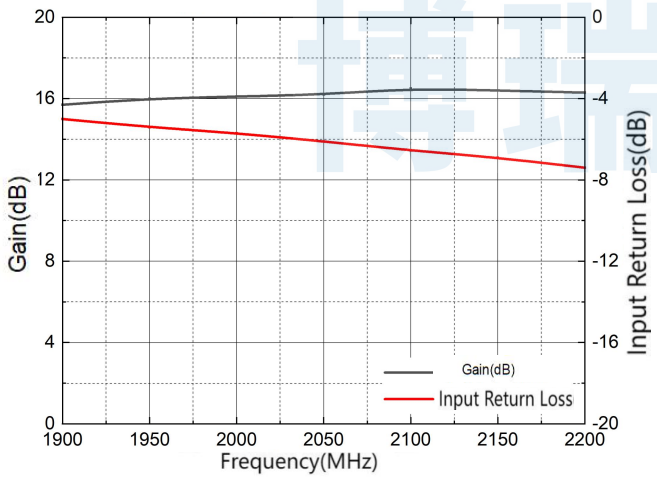
ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

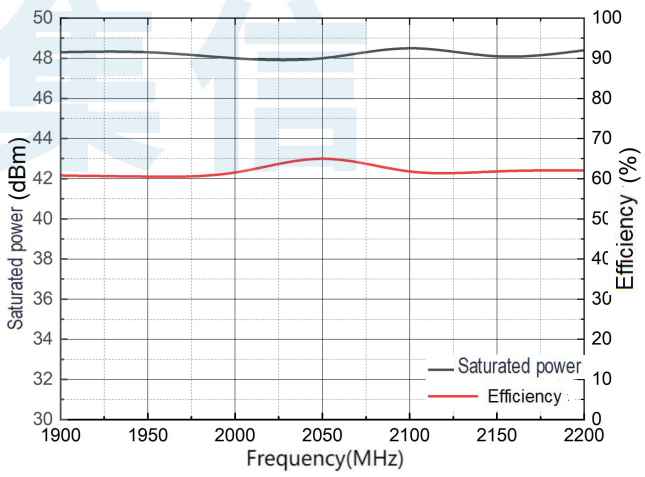
Rf Characteristics: Evaluation Board (1.9GHz ~ 2.2GHz) Test Data

Parameters	Typ.							Units
Frequency	**1900**	**1950**	**2000**	**2050**	**2100**	**2150**	**2200**	MHz
Gain	15.7	16.0	16.1	16.2	16.5	16.4	16.3	dB
Small Signal Input Return	-5.0	-5.4	-5.7	-6.1	-6.6	-6.9	-7.4	dB
Drain Current @P_{sat}	3.74	3.77	3.45	3.25	3.87	3.53	3.82	A
Output Power @P_{sat}	48.3	48.3	48.0	48.0	48.5	48.1	48.4	dBm
Power Gain @P_{sat}	12.6	12.7	12.5	12.1	12.7	12.7	13.9	dB
PAE@P_{sat}	60.88	60.53	61.55	64.98	61.82	61.82	62.06	%
Test Conditions: Temp =+25℃V_{DD}, =+28V, =I_{DQ}300mA, CW test; Note: defined as the saturation P_{sat}power output of the evaluation board.								

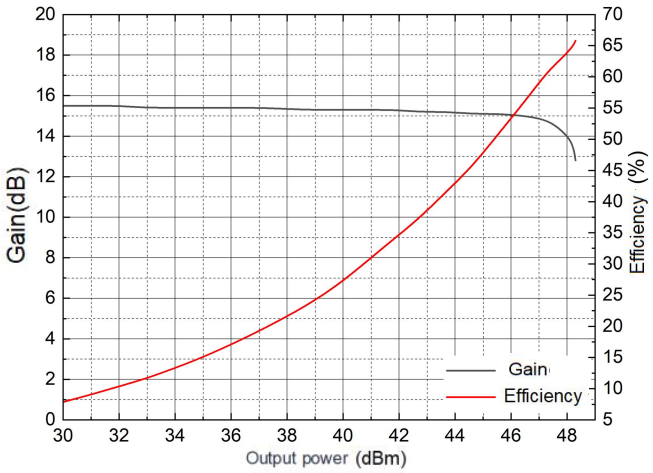
Typical Performance (Evaluation board: 1.9GHz-2.2GHz, Temp =+25℃, =+28V, =300mA, CW wave test$V_{DD}$$I_{DQ}$)



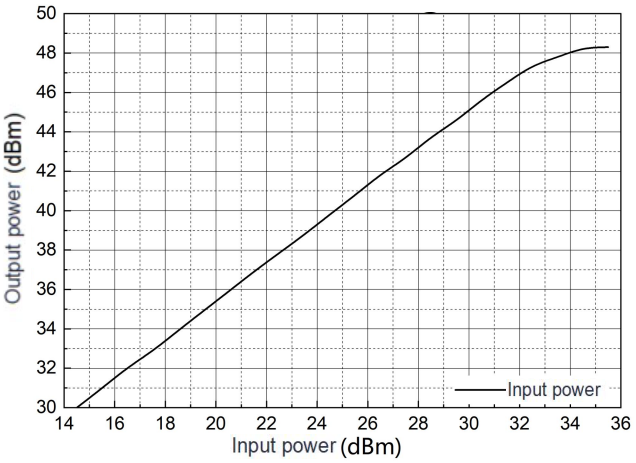
Input Return, Gain vs Freq



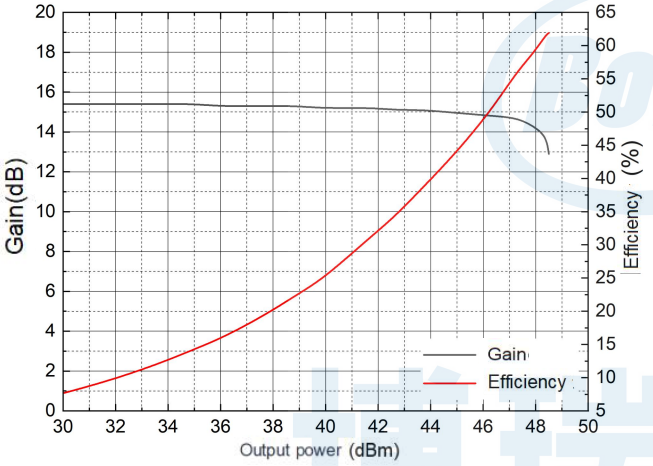
Saturation Power, Efficiency, vs Freq



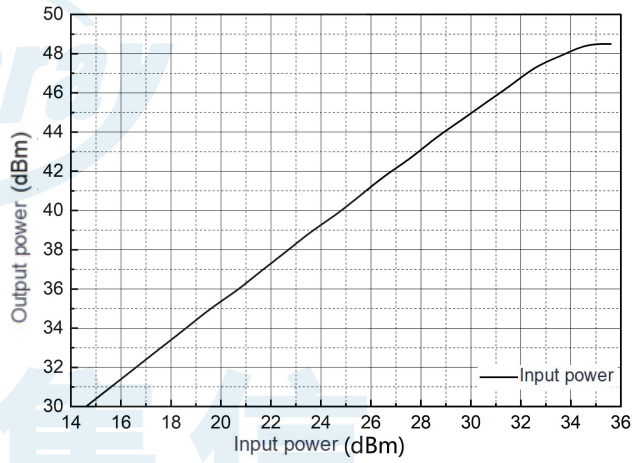
Gain, Added Efficiency vs P_{out}@2GHz



P_{out} vs Pin@2GHz

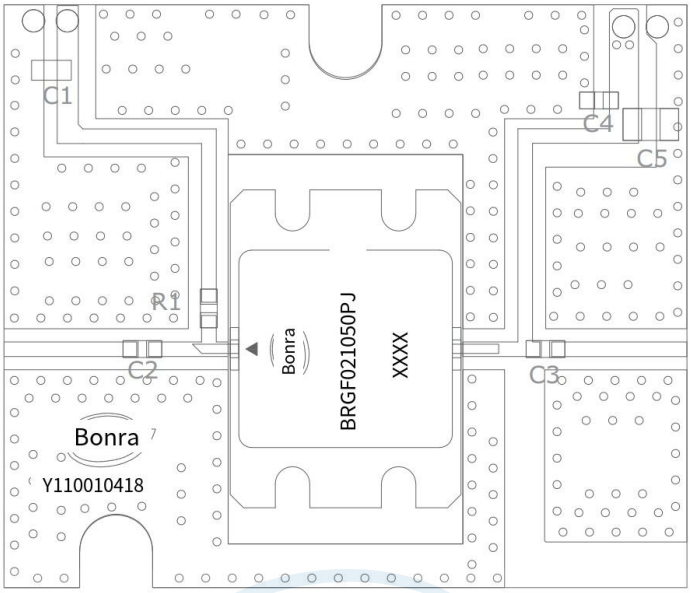


Gain, Added Efficiency vs P_{out} @2.1GHz

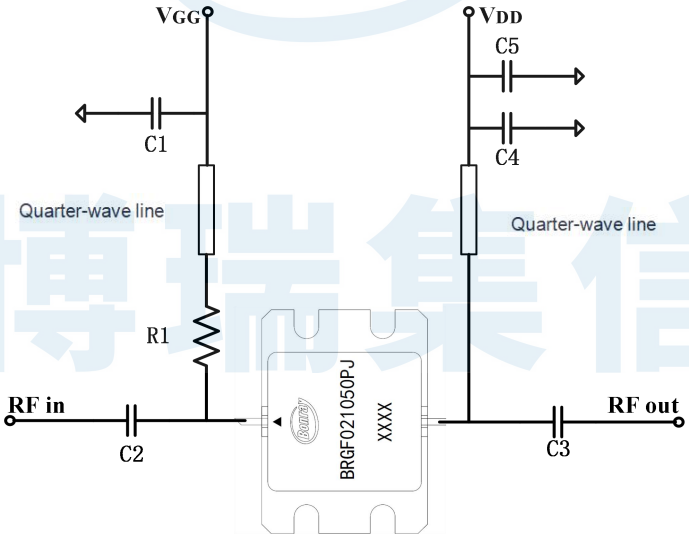


P_{out} vs Pin@2.1GHz

Typical Application Schematic



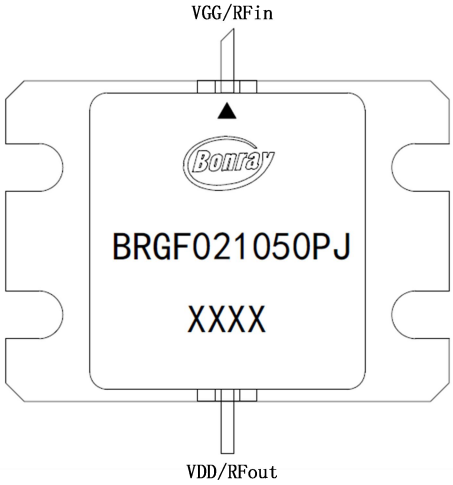
Assembly Diagram



Bill of Material

Designator	Package	Value	Part Number
C2,C3,C4	0805	100pF	VJ0805D101JXPAJ
C1	1206	4.7 uF	GRM31CC72A475KE11#
C5	1210	10uF	GRM32EC72A106KE05#
R1	0805	30ohm	CRT0805-FX-30R0ELF

Pin Configuration and Description



Pin Number	Pin Name	Description
1	VGG/Rfin	Gate, gate voltage regulation, RF signal 50Ω system input
2	VDD/Rfout	Drain, drain voltage input, RF power signal 50Ω system output
-	Package Base	Device housing, to be welded or well coated on the bottom Mount to the heat dissipation and ground network substrate to ensure good heat dissipation and RF grounding

Power-on Sequence

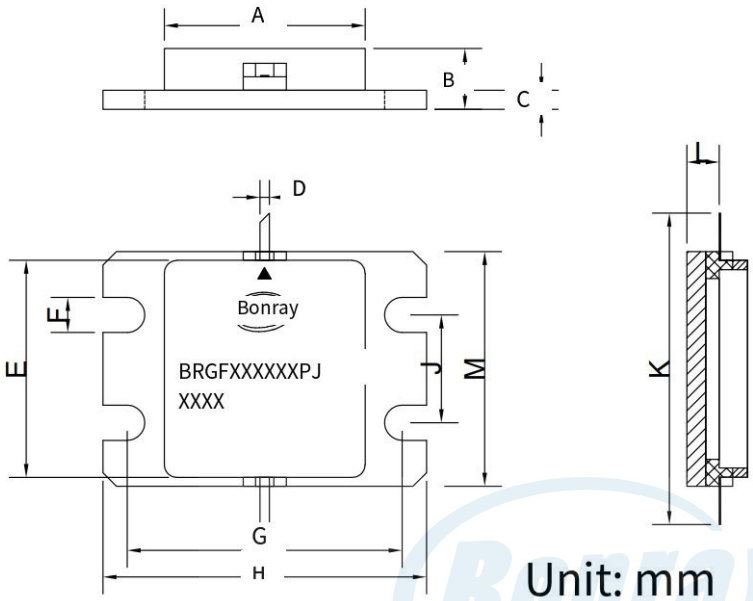
1. Set the gate voltage (V_{GG}) to -5V;
2. Set drain voltage (V_{DD}) to +28V, current limit 6A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 300mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal;
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off the drain Supply Voltage voltage;
4. Turn off the gate Supply Voltage voltage;

Note: When the circuit is designed, the offset voltage needs to have a timing protection circuit to ensure that it is fully powered on before adding, and ensure that it is reduced to below 5V when powering off, before starting to power off; $V_{GG}V_{DD}V_{DD}V_{GG}$Especially in TDD Application, gate Supply Voltage decoupling capacitors need to be rigorously evaluated to meet switching speed requirements.

Package Dimensions (mm)



DIM	MILIMETER		DIM	MILIMETER	
	MIN.	MAX		MIN.	MAX
A	14.77	15.03	G	20.27	20.53
B	4.3	47	H	23.85	24.15
C	1.27	1.53		7.87	8.13
D	0.6	0.8	K	26.2	26.8
E	15.97	16.23	L	2.25	2.55
F	2.6		M	17.25	

Unit: mm

Recommended Soldering Temperature Profile