Product Features

Operating Frequency: 0.02GHz ~ 8GHz

Gain: 16.3dB@4GHz

Output Power for 1dB Compression:

20.1dBm@4GHz

Noise Figure: 3.3dB@4GHz

Output Third-Order Interception:

34.1dBm@1GHz

+5V Single Power Supply

Supply Current:

97mA@ Vdd=+5 (Normal Operation Mode)

62mA@ Vdd=+5 (Low-power Operation Mode)

Die Size: 950um x 850um x 100um

Application

Radio Communication

Communication Base Station

Testing and Measuring Equipment

Radar and Electronic Countermeasures

Navigation Equipment

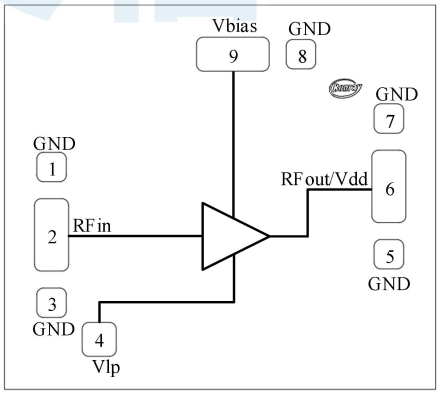
Ordering Information

Part Number	Package	Description
BR9641LDZ	Die	0.02GHz~ 8GHz Gain Block Amplifier

General Description

BR9641LDZ is a broadband high-performance MMIC gain amplifier designed using GaAs process. Covering a frequency range of 0.02GHz~8GHz, the amplifier is internally matched to 50 ohms, and only require an external RF choke and blocking/bypass capacitors. The amplifier contains on-chip active bias network to ensures that the quiescent current is not affected by temperature. The amplifier has the characteristics of high gain flatness and high linearity when powered by a single supply operation of +5V in normal operation mode. The product is also compatible with low-power operation mode to meet the requirements of applications with stringent power consumption demands.

Functional Block Diagram



Electrical Specifications

Parameter	Min.	Typ.	Max.	Units	Test Conditions
Gain	-	18.1	-	dB	20MHz
	-	16.3	-	dB	4000MHz
	-	17.1	-	dB	8000MHz
Output Power for 1dB Compression	-	18.5	-	dBm	20MHz
	-	20.1	-	dBm	4000MHz
		15.9		dBm	8000MHz
Output Third-Order Interception	-	31.7	-	dBm	20MHz
	-	29.5	-	dBm	4000MHz
		26.1		dBm	8000MHz
Noise Figure	-	2.9	-	dB	20MHz
		3.3		dB	4000MHz
		4.6		dB	8000MHz
Input Return Loss	-	-11.9	-	dB	20MHz
		-18.7		dB	4000MHz
		-9.5		dB	8000MHz
Output Return Loss	-	-16.6	-	dB	20MHz
		-15.9		dB	4000MHz
		-11.1		dB	8000MHz
Reverse Isolation	-	-23.2	-	dB	4000MHz
Supply Voltage	-	+5	-	V	-
Supply Current	-	97	-	mA	-
Test Conditions: Vdd=+5V, Idd=97mA, OIP3 spacing=1MHz, Pout=5dBm/tone, TA=+25℃					

Absolute Maximum Ratings

Recommended Operating Conditions

Maximum Supply Voltage (Vdd): +6V

Maximum RF input Power: +21dBm

Supply Voltage: +5V

Supply Current:

97mA @ Vdd=5V (Normal Operation Mode)

62mA @ Vdd=5V (Low-power Operation Mode)

Storage Temperature: -65℃ ~ +150℃

Operating Temperature: -55℃ ~ +125℃

Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and exposure to absolute-maximum-ratings conditions for extended periods will affect the reliability.

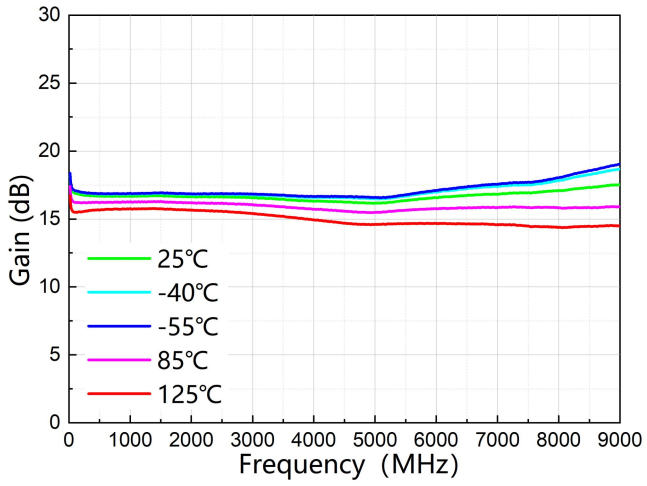
ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

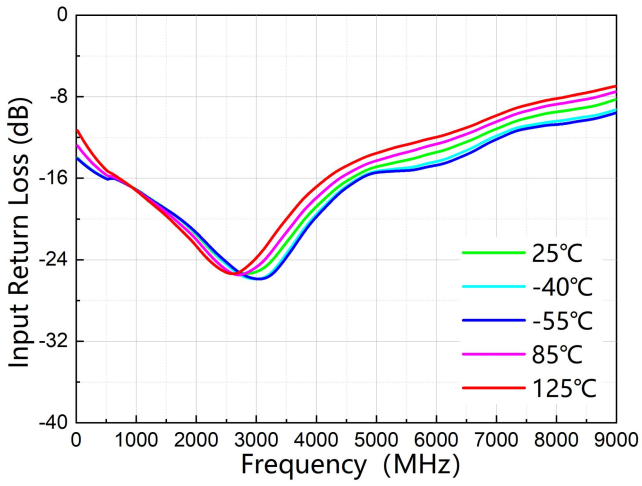
OBSERVE HANDLING PRECAUTIONS

Typical Performance (EVB test results at +5V supply voltage in normal operation mode)

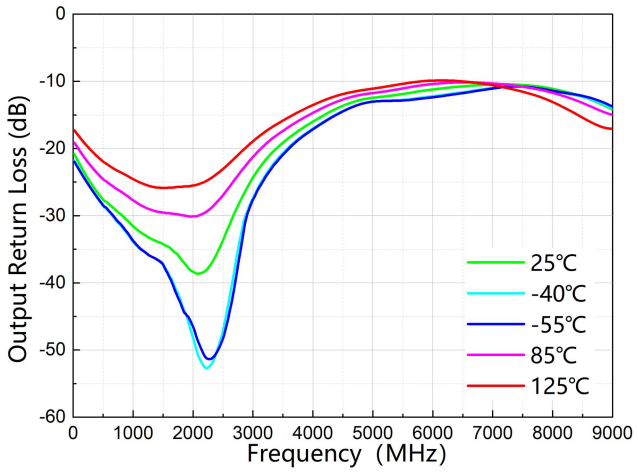
Parameter	Typ.											Units
Frequency	20	50	100	200	400	600	800	1000	1500	2000	2500	MHz
Gain	18.1	17.1	16.9	16.8	16.7	16.7	16.7	16.7	16.7	16.6	16.7	dB
Input Return Loss	-11.9	-12.9	-14.5	-15.8	-15.7	-16.0	-16.5	-17.1	-19.1	-21.6	-24.5	dB
Output Return Loss	-16.6	-20.9	-23.1	-24.2	-26.8	-28.2	-29.9	-31.5	-34.0	-37.9	-33.8	dB
Reverse Isolation	-22.0	-21.6	-21.9	-21.7	-22.2	-22.0	-22.1	-22.1	-22.2	-22.2	-22.5	dB
Output Power for 1dB Compression	18.5	18.9	19.6	20.3	20.8	21.0	21.0	21.1	21.1	21.0	20.9	dBm
Output Third-Order Interception	31.7	32.3	32.8	33.4	34.3	34.5	34.4	34.1	33.7	32.8	32.0	dBm
Noise Figure	2.9	3.2	3.2	3.2	3.0	3.0	3.0	3.0	3.0	3.0	3.1	dB
Frequency	3000	3500	4000	4500	5000	5500	6000	6500	7000	7500	8000	MHz
Gain	16.6	16.4	16.3	16.2	16.2	16.4	16.6	16.7	16.8	16.9	17.1	dB
Input Return Loss	-25.3	-22.3	-18.7	-16.3	-14.9	-14.3	-13.4	-12.4	-11.1	-10.1	-9.5	dB
Output Return Loss	-24.4	-19.2	-15.9	-13.7	-12.4	-11.9	-11.3	-10.8	-10.4	-10.5	-11.1	dB
Reverse Isolation	-22.6	-22.9	-23.2	-23.4	-23.8	-23.9	-24.2	-24.4	-25.0	-25.1	-25.7	dB
Output Power for 1dB Compression	20.7	20.3	20.1	19.9	19.4	18.5	17.5	17.1	17.0	16.5	15.9	dBm
Output Third-Order Interception	31.2	30.3	29.5	29.0	28.5	28.1	27.9	27.7	27.5	27.0	26.1	dBm
Noise Figure	3.1	3.2	3.3	3.4	3.4	3.3	3.5	3.8	4.1	4.4	4.6	dB
Test Conditions: Vdd=+5V, Idd=97mA; OIP3 spacing=1MHz, Pout=5dBm/tone; TA=+25°C												



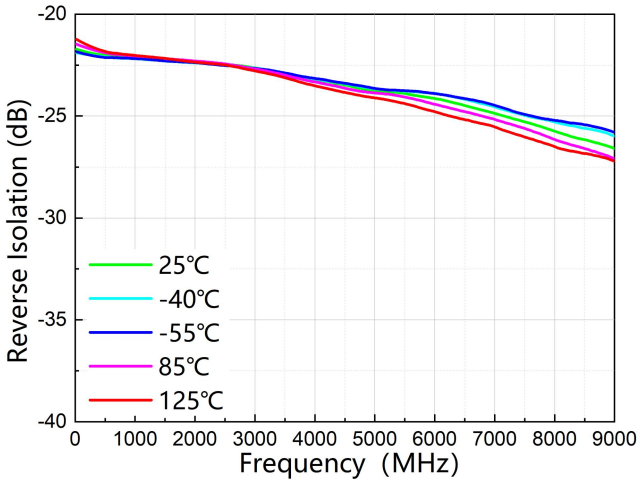
Gain vs. Freq



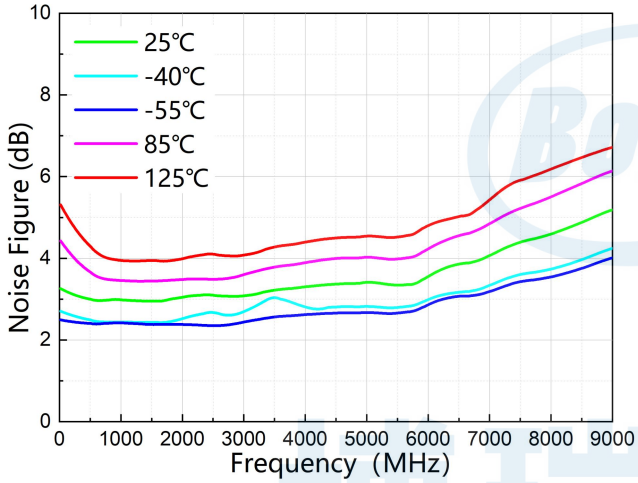
Input Return Loss vs. Freq



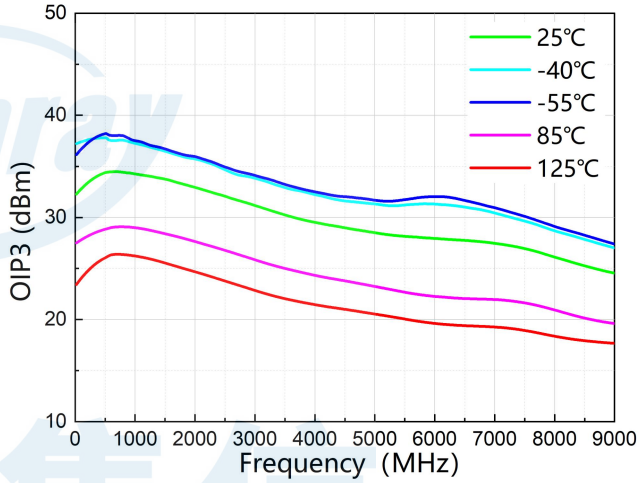
Output Return Loss vs. Freq



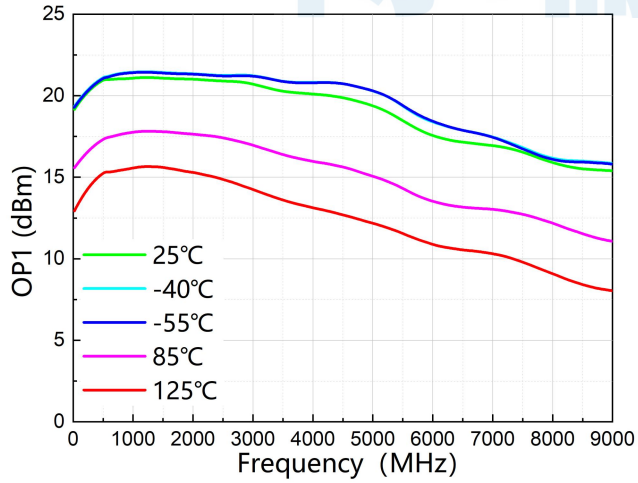
Reverse Isolation vs. Freq



Noise Figure vs. Freq



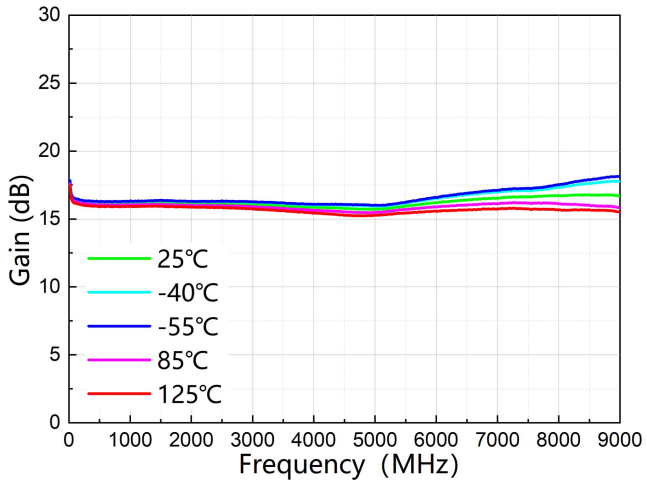
Output Third-Order Interception vs. Freq



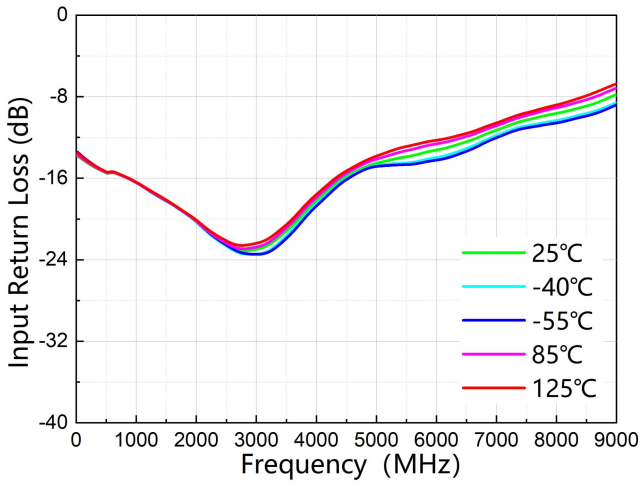
Output Power for 1dB Compression vs. Freq

Typical Performance (EVB test results at +5V Supply voltage in low-power operation mode)

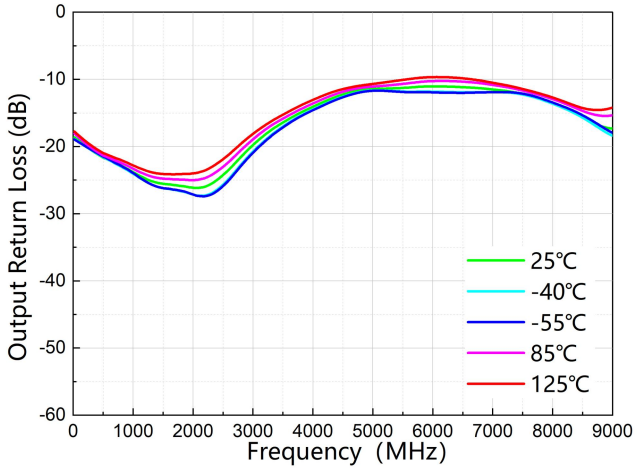
Parameter	Typ.											Units
Frequency	20	50	100	200	400	600	800	1000	1500	2000	2500	MHz
Gain	17.7	16.7	16.4	16.3	16.2	16.2	16.2	16.2	16.2	16.2	16.2	dB
Input Return Loss	-11.8	-12.7	-14.2	-15.3	-15.2	-15.4	-15.9	-16.5	-18.3	-20.4	-22.6	dB
Output Return Loss	-16.1	-18.6	-19.4	-19.9	-21.2	-22.0	-22.9	-23.8	-25.7	-26.2	-24.5	dB
Reverse Isolation	-21.2	-21.7	-22.0	-21.7	-21.7	-21.9	-21.9	-21.9	-22.1	-22.3	-22.3	dB
Output Power for 1dB Compression	18.7	19.3	20.1	20.2	20.4	20.3	20.4	20.4	20.3	20.2	19.9	dBm
Output Third-Order Interception	32.0	32.6	33.5	33.5	33.8	34.0	33.9	34.0	33.6	33.4	33.0	dBm
Noise Figure	2.9	3.2	3.2	3.2	3.0	3.0	3.0	2.9	2.9	3.0	2.9	dB
Frequency	3000	3500	4000	4500	5000	5500	6000	6500	7000	7500	8000	MHz
Gain	16.1	16.0	15.9	15.8	15.7	16.0	16.2	16.4	16.5	16.6	16.7	dB
Input Return Loss	-23.1	-21.2	-18.2	-15.8	-14.6	-13.9	-13.2	-12.4	-11.3	-10.3	-9.6	dB
Output Return Loss	-19.8	-16.4	-14.1	-12.2	-11.4	-11.3	-11.1	-11.2	-11.5	-12.1	-13.4	dB
Reverse Isolation	-22.5	-23.0	-23.1	-23.4	-23.7	-23.9	-24.0	-24.4	-24.7	-24.8	-25.4	dB
Output Power for 1dB Compression	19.6	19.0	18.6	18.2	17.8	17.6	17.8	17.8	17.8	17.1	16.4	dBm
Output Third-Order Interception	32.4	31.3	30.5	30.2	30.1	30.3	31.1	32.2	33.8	36.3	35.7	dBm
Noise Figure	3.0	3.2	3.2	3.3	3.3	3.2	3.4	3.6	3.8	4.1	4.3	dB
Test Conditions: Vdd=+5V, Idd=62mA; OIP3 spacing=1MHz, Pout=5dBm/tone; TA=+25°C												



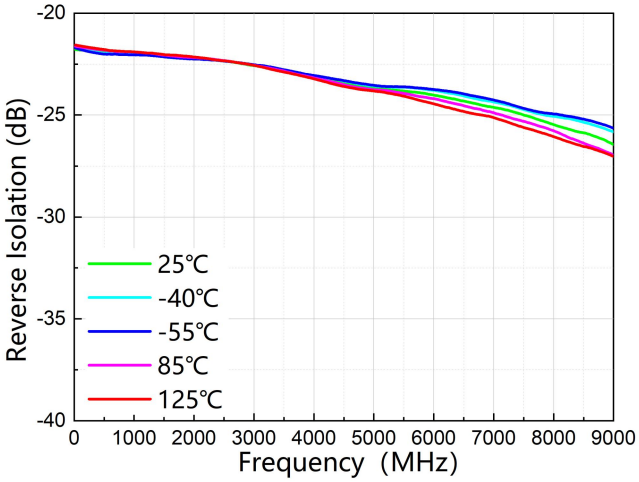
Gain vs. Freq



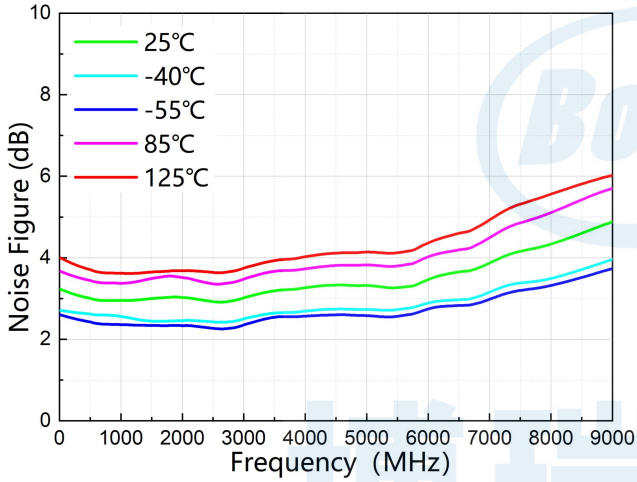
Input Return Loss vs. Freq



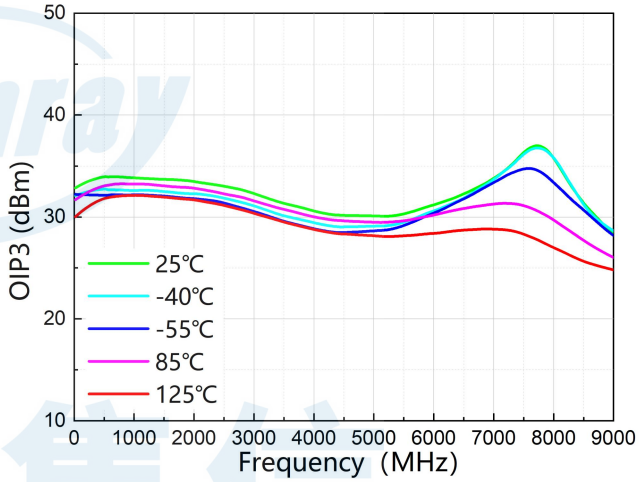
Output Return Loss vs. Freq



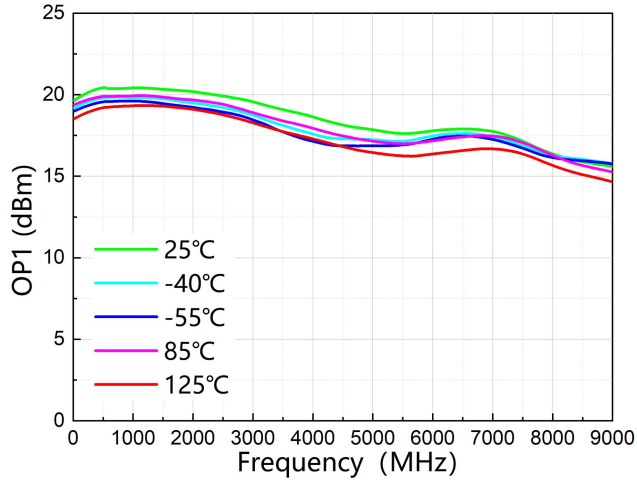
Reverse Isolation vs. Freq



Noise Figure vs. Freq

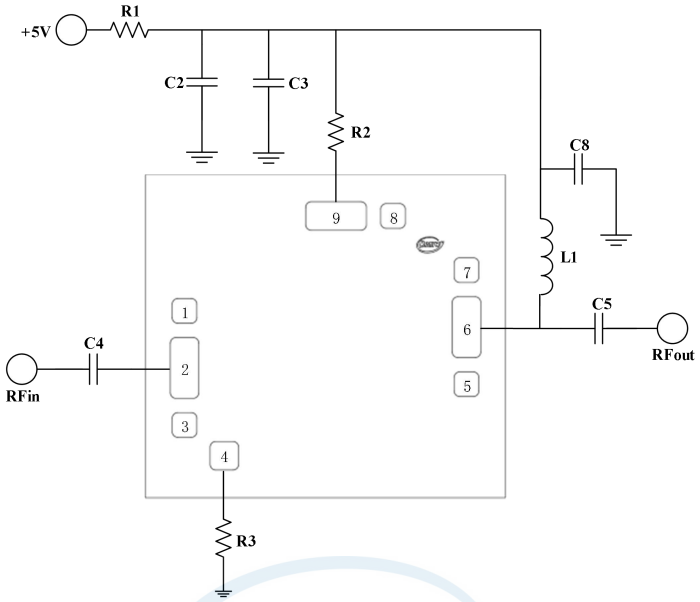


Output Third-Order Interception vs. Freq



Output Power for 1dB Compression vs. Freq

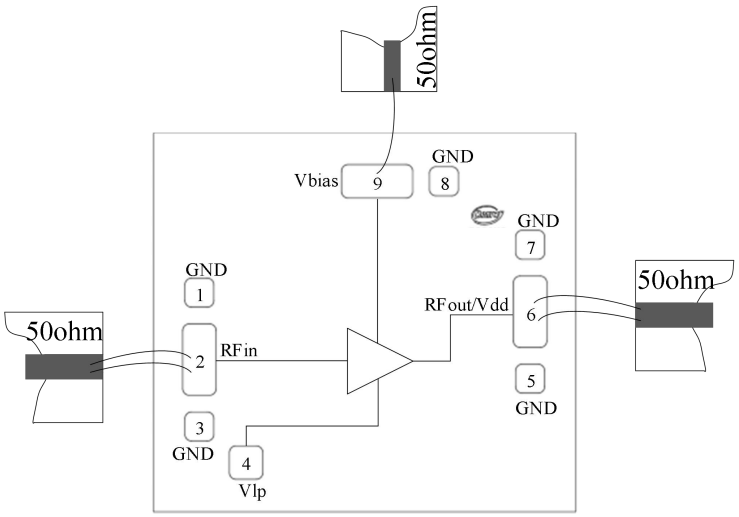
Typical Application Schematic



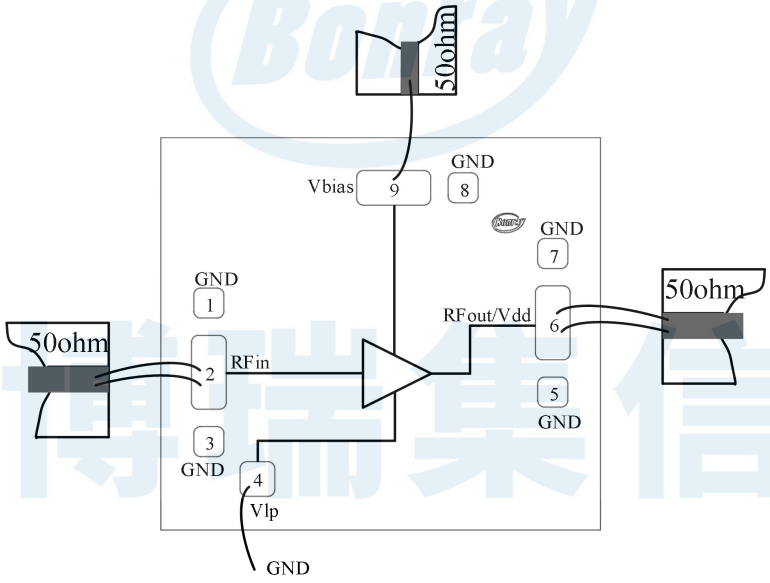
Bill of Material

Reference Designator	Package Size	Value	P/N
U1	Naked Die	0.02GHz~8GHz Gain Block Amplifier	BR9641LDZ
L1	1008	1.1uH	1008AF-112XJRB
C2	0402	100nF	GRM155R71H104KE14D
C3, C8	0402	10nF	GRM155R71H103JA88D
C4	0402	3.3nF	GRM155R71H332JA01D
C5	0402	330pF	GRM1555C1H331JA01D
R1	0402	0Ω	RC0402FR-070RL
R2	0402	5.6Ω	RC0402JR-075R6L
R3 (Normal operation mode)	/	Idle	/
R3 (low-power operation mode)	0402	0Ω	RC0402JR-070RL

Assembly Diagram



Assembly diagram for normal operation Mode



Assembly diagram for low-power operation mode

Note: Refer to typical application schematic and bill of material for external components

Handling Precautions：

1. **Storage:** All bare dies are placed in ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

2. Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

3. Electrostatic protection: Follow ESD precautions to protect against ESD strikes.

4. Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pickup.

5. General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip should not be touched with vacuum collet, tweezers, or fingers.

6. Mouning: The chip is back-metallized and can be die mounted with electrically conductive epoxy. The mounting surface should be clean and flat.

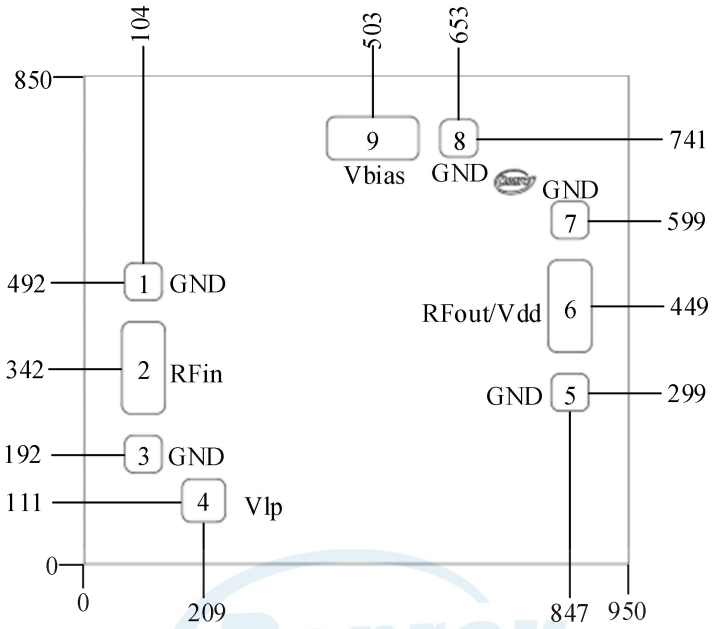
7. Conductive epoxy Die Attach: Apply conductive epoxy to the mounting surface so that the overflow of conductive epoxy on all four sides should not be less than 75%, and the height of conductive epoxy climbing on all four sides should not exceed the surface of the chip. Cure conductive epoxy per the manufacturer's schedule

8. **Bonding process**: Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. **The arc height of all bonds is 6mil (reference value). The projected length of RFin bond is 857um (reference value), RFout/Vdd bond 848um (reference value), Vbias bond 676um (reference value), and Vlp bond 1300um (reference value) in low-power operation mode.**

9. **Die bonding void rate**: not more than 10%.

10. Please contact customer service if you have any problem.

Mechanical Information (Units: um)



Notes:

1. Backside and bond pad metal: Gold;
2. Backside is RF and DC ground;
3. Pads size: RFin 75um×160um, RFout/Vdd 75um×160um, Vbias 75um×160um, Vlp 75um×75um, GND 65um×65um;
4. Cannot be bonded on the hole.

Functional Description

Pad	Function	Description
2	RFin	RF Input. A DC Block is required.
6	RFout/Vdd	RF Output. DC bias will also need to be injected through a RF bias choke/inductor for operation.
1, 3, 5, 7, 8	GND	Connected to die bottom through hole
9	Vbias	Sets the Icq bias point for the device.
4	Vlp	Sets operation modes, and see assembly for required operation mode
Die Bottom	GND	Die bottom must be well grounded to RF/DC