Product Features

Frequency: 0.01GHz ~ 2.8GHz

Gain : 19.1dB@1GHz

Psat: 40.7dBm@1GHz

PAE: 50.4%@1GHz

V_{DD}=28V, I_{DQ} 100mA

Package: QFN32 (5mm×5mm)

Application

Power Amplification Stage Suitable for Wireless Infrastructure

Test and Measure Equipment

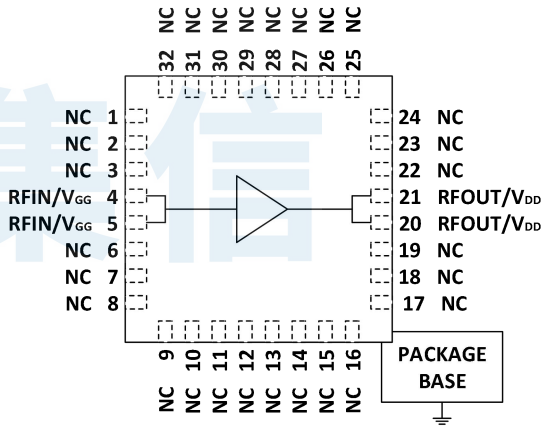
Commercial and Military Radars

General Transmitter Applications

General Description

The BR9274FL is a gallium nitride (GaN) wideband transistor capable of delivering 10W (40dBm) output from 10MHz to 2.8GHz at an input power of 27dBm, with a power PAE up to 55% and a small signal Power Gain flatness of 3dB. The BR9274FL is ideal for pulse or continuous-wave applications such as wireless infrastructure, radar, public mobile radio communications and general-purpose amplification.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BR9274FL	QFN32	10MHz to 2.8GHz GaN Amplifier

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain Current (I_D)	1.5 A
Gate Current (I_G))	6mA
Continuous Dissipated Power (P_D)	25W
Channel Temperature (T_{CH})	275 ℃
Mounting Temperature (30 seconds)	245 ℃

Note: Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Numerical values
Drain Voltage (V_{DD})	+28V
Drain Static Current (I_{DQ})	100mA
Peak Drain Current (I_D)	1.2 A
Gate Voltage (V_{GG})	2.46 V
Channel Temperature (T_{CH})	225 ℃
Continuous Dissipated Power CW (P_D)	20W (25 ° C)
Storage Temperature	-65℃ ～+150℃
Operating Temperature	-55℃ ～+85℃
ESD Rating	Class 1A

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Thermal Parameters

Parameters	Test Condition	Value	Units
Thermal resistance (θ_{JB})	DC at 85 ° C case	10	°C/W

Note:θ_{JB} is the thermal resistance measured from GaN core to the back of PCB;

ESD WARNING

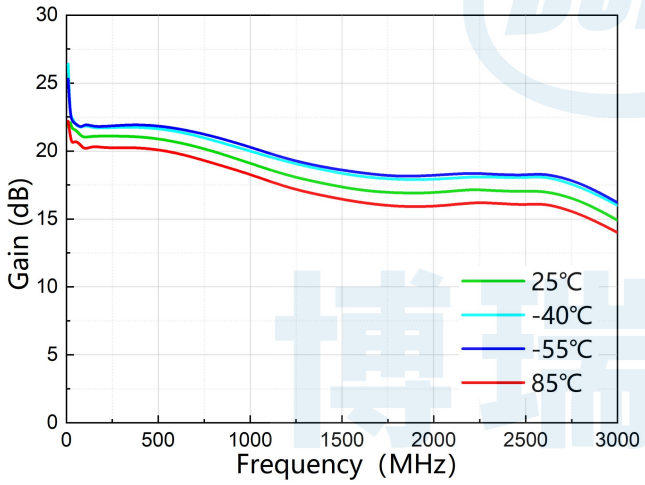
ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

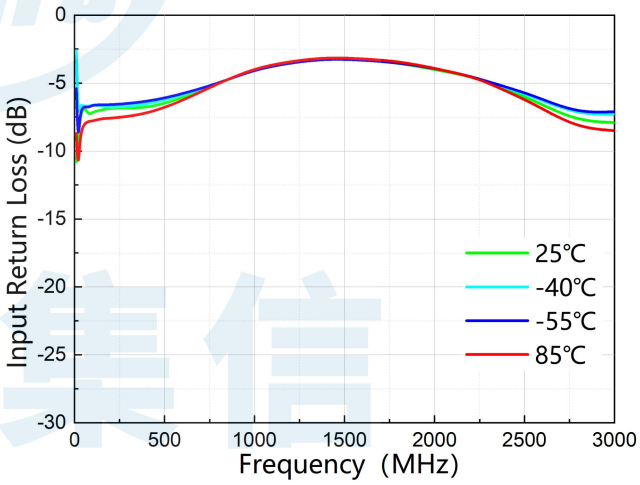
Typical Performance (EVB test results: 0.01GHz~2.8GHz)

Parameters	Typ.									Units
Frequency	10	30	100	600	1000	1500	2000	2500	2800	MHz
Gain	21.8	21.6	21.0	20.7	19.1	17.4	16.9	17.0	16.4	dB
Input Return Loss	-10.8	-7.7	-7.1	-6.1	-4.0	-3.3	-4.0	-6.0	-7.8	dB
Output Return Loss	-13.8	-18.4	-15.9	-9.4	-9.6	-8.5	-9.8	-10.0	-7.6	dB
P1dB	22.9	26.7	26.1	24.9	22.9	21.3	23.3	26.2	34.5	dBm
OIP3	47.3	52.6	51.9	52.5	50.3	51.0	49	48.3	49.6	dBm
Psat	41.0	40.8	41.4	40.8	40.7	41.3	41.8	41.8	40.7	dBm
PAE @Psat	61.5	65.8	65.6	54.8	50.4	45.2	45.7	53.5	44.1	%
Test Conditions: V_{DD}=28V, I_{DQ}=100mA, OIP_3 spacing=1MHz/Tone, Pout=30dBm/tone, TA=+25°C										

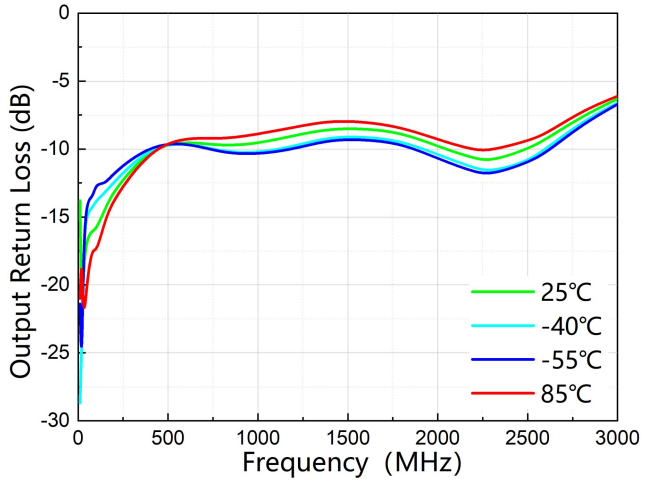
Typical Performance (V_{DD}=28V, EVB test result: 10MHz~2.8GHz)



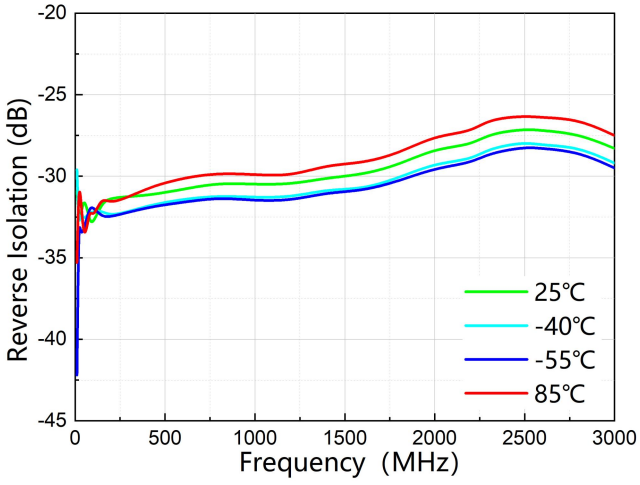
Gain vs. Freq



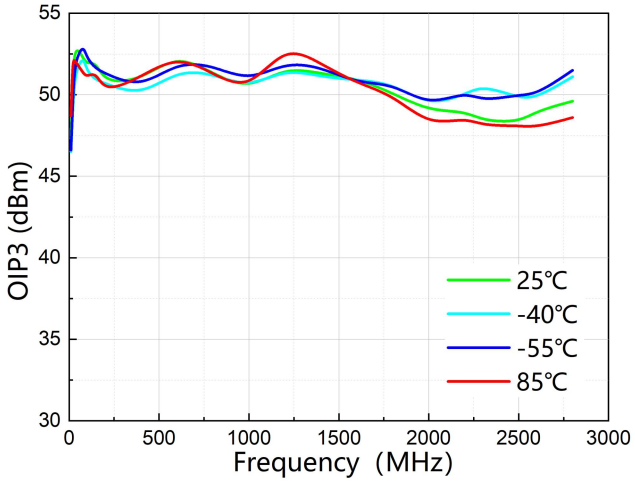
Input Return Loss vs. Freq



Output Return Loss vs. Freq

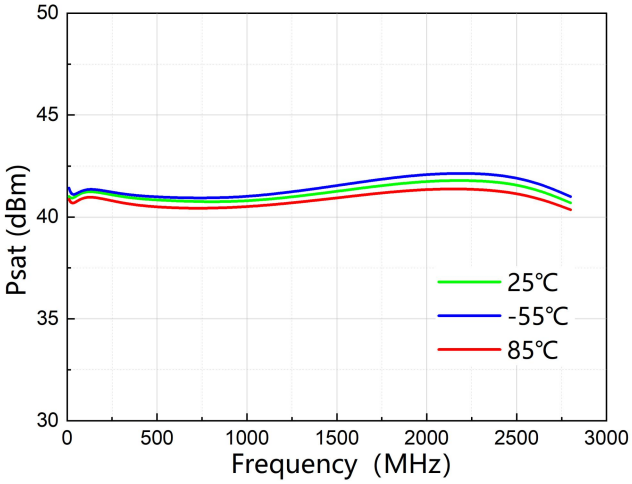


Reverse Isolation vs. Freq

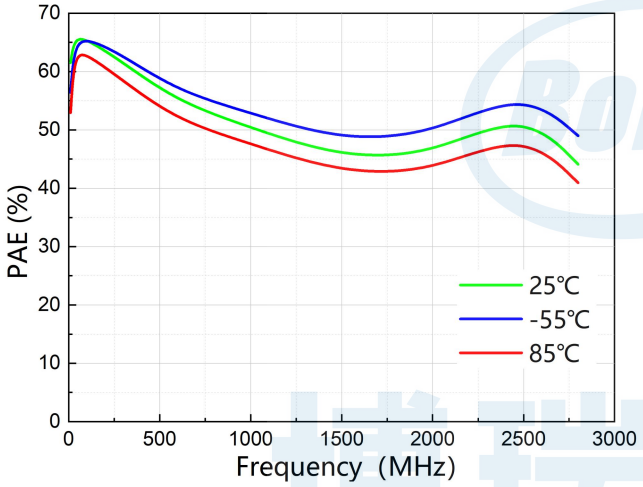


Output Third-Order Interception vs. Freq

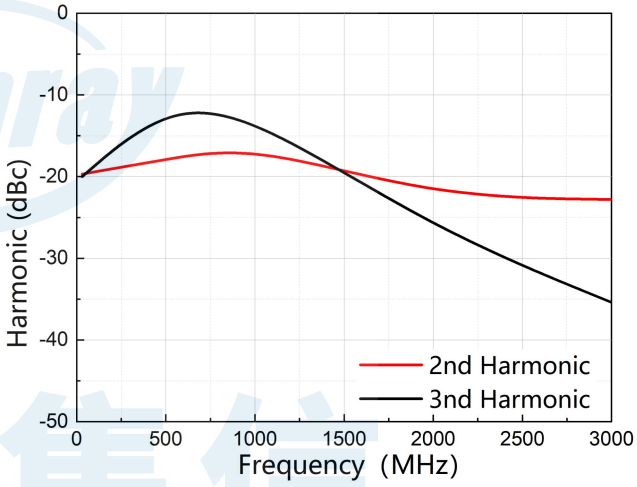
Spacing=1MHz, Pout=30dBm/tone



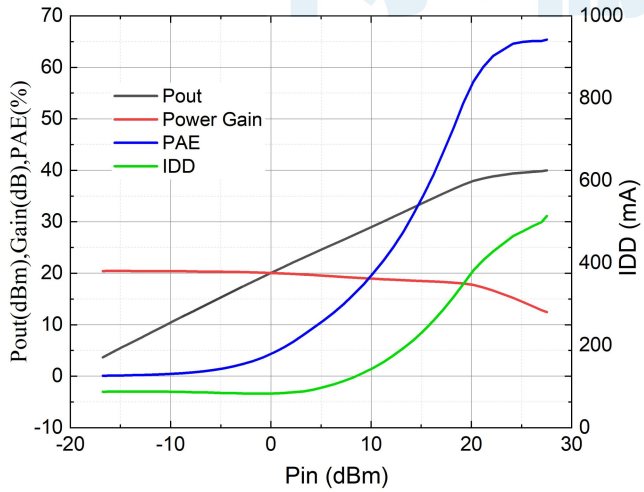
Psat vs. Freq



PAE@Psat vs. Freq

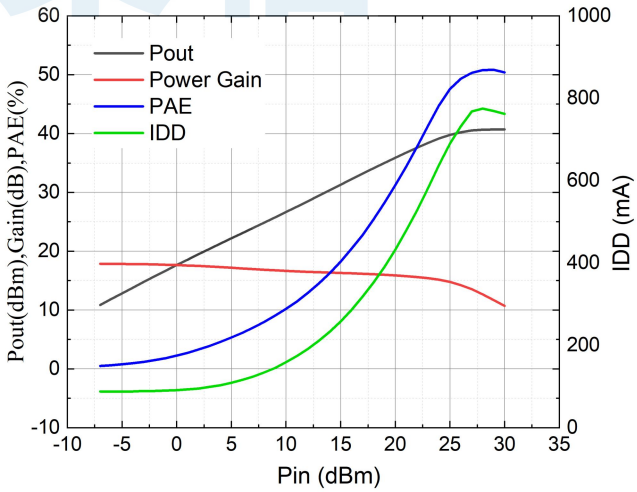


Second/Third Harmonics @Psat vs. Freq



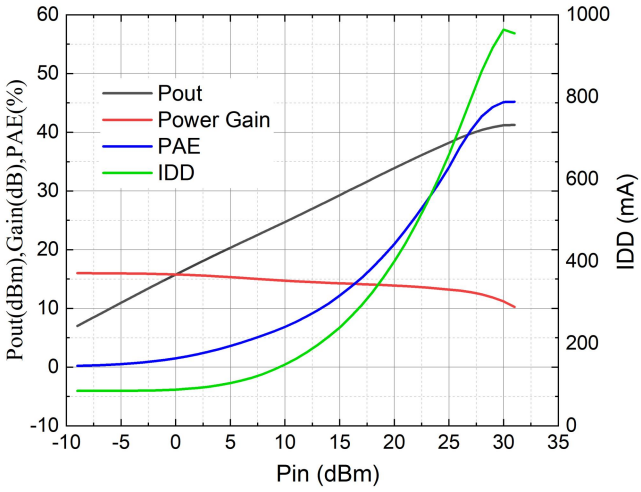
Pout &Power Gain&PAE&IDD vs.Pin

@100MHz

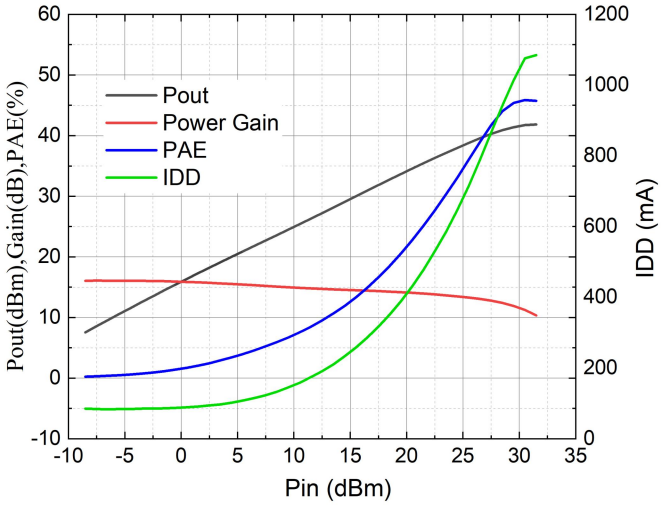


Pout &Power Gain&PAE&IDD vs.Pin

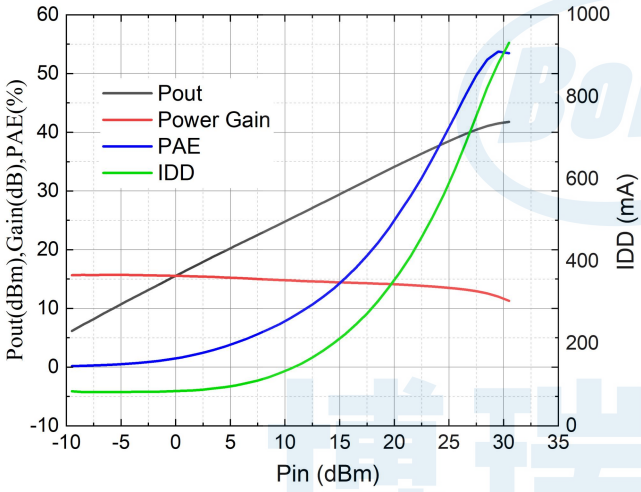
@1GHz



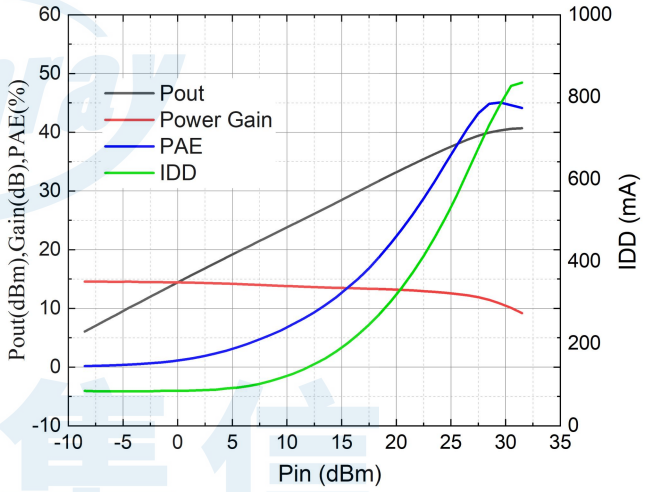
Pout &Power Gain&PAE&IDD vs.Pin @ 1.5 GHz



Pout &Power Gain&PAE&IDD vs.Pin @2GHz

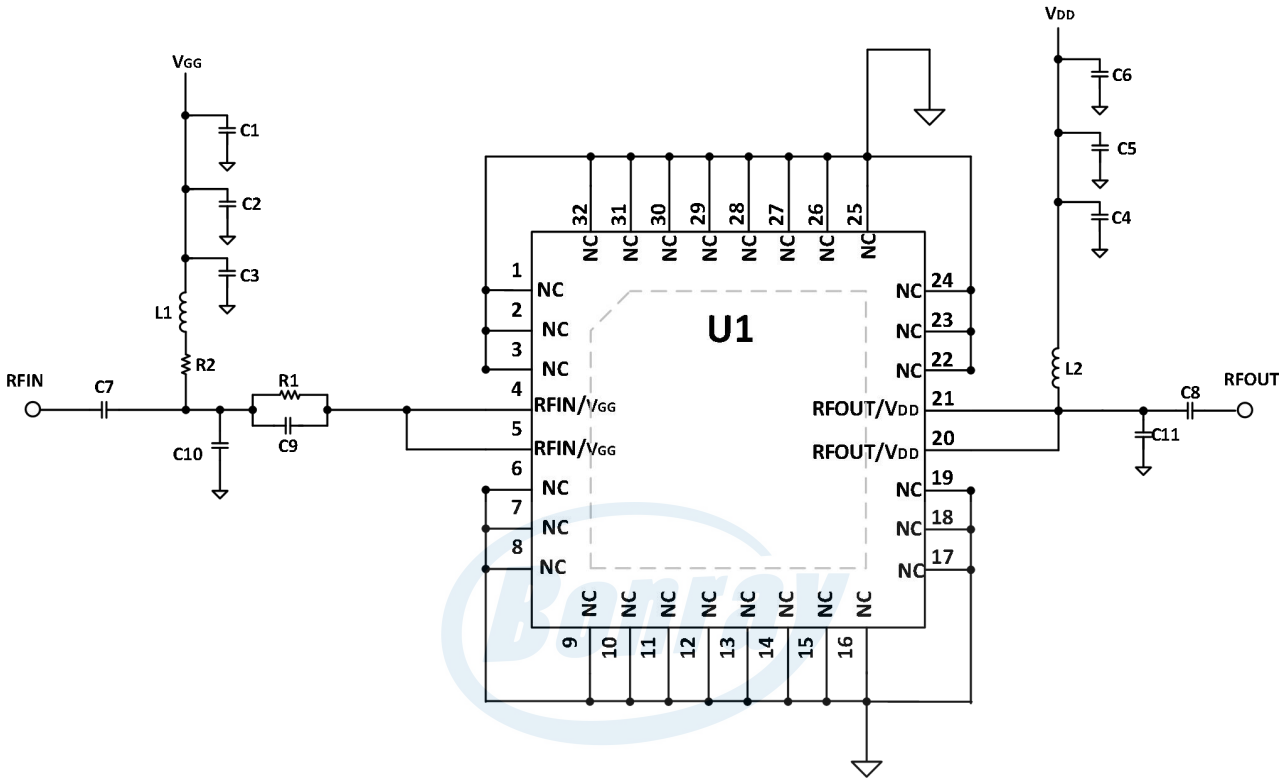


Pout &Power Gain&PAE&IDD vs.Pin @ 2.5 GHz



Pout &Power Gain&PAE&IDD vs.Pin @ 2.8 GHz

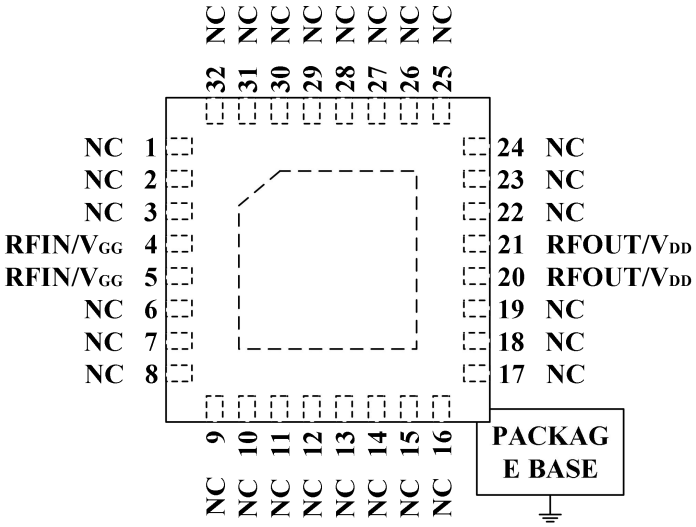
Typical Application Schematic



Bill of Material

Designator	Package	Description	Part Number
U1	QFN32	10W GaN broadband power amplifier	BR9274FL
L1	0603	6.8 nH	LQW18AN6N8G80
L2	1008	1.1 uH	1008AF-112XJRB
C1, C2, C5, C6	1210	10uF	GRM32ER71H106KA12L
C3, C4, C7, C8	0603	2.2 the nF	GRM1885C1H222JA01D
R1	0603	15 Ω	RC0603JR-0715RL
R2	0603	43 Ω	RC0603FR-0743RL
C9	0603	200pF	0603B201K500NT
C10	0603	1.2 pF	GRM1885C2A1R2BA01
C11	0603	0.75 PF	GQM1875C2ER75BB12

Pin Configuration and Description



Pin Number	Pin Name	Description
1, 2,3, 6 to 19, 22 to 32	NC	The interior is not connected, in the test these ports need to be connected to the external RF ground or DC ground to achieve good heat dissipation effect.
4, 5	RFIN/V_{GG}	Rf input/gate bias voltage, to be externally matched to 50ohm.
20, 21	RFOUT/V_{DD}	The RF output/drain bias voltage must be externally matched to 50ohm.
-	EP	Exposed pads, exposed pads must be connected to RF ground and DC ground.

Power-on Sequence

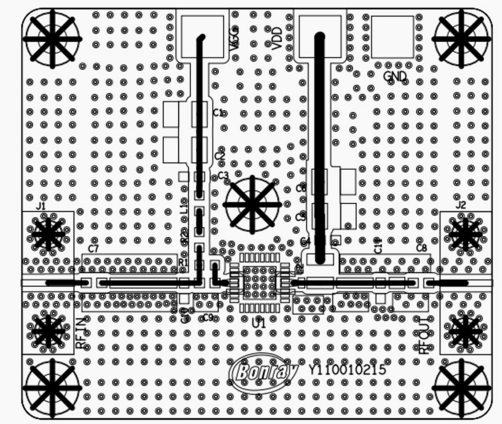
1. Set the gate voltage (V_{GG}) to -5V
2. Set drain voltage (V_{DD}) to +28V, current limit 1200mA
3. Turn on the gate voltage
4. Turn on drain voltage
5. Increase the gate voltage (V_{GG}) so that the drain current is 100mA
6. Input RF signal

Power-off Sequence

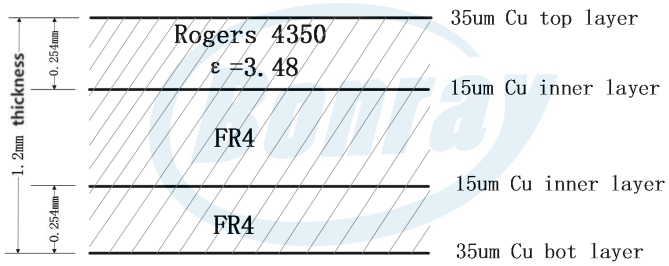
1. Turn off the RF signal
2. Reduce the gate voltage (V_{GG}) to -5V
3. Turn off the drain Supply Voltage voltage
4. Turn off the Supply Voltage voltage of the gate

Note: **:** In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before VGG is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

PCB Evaluation Board

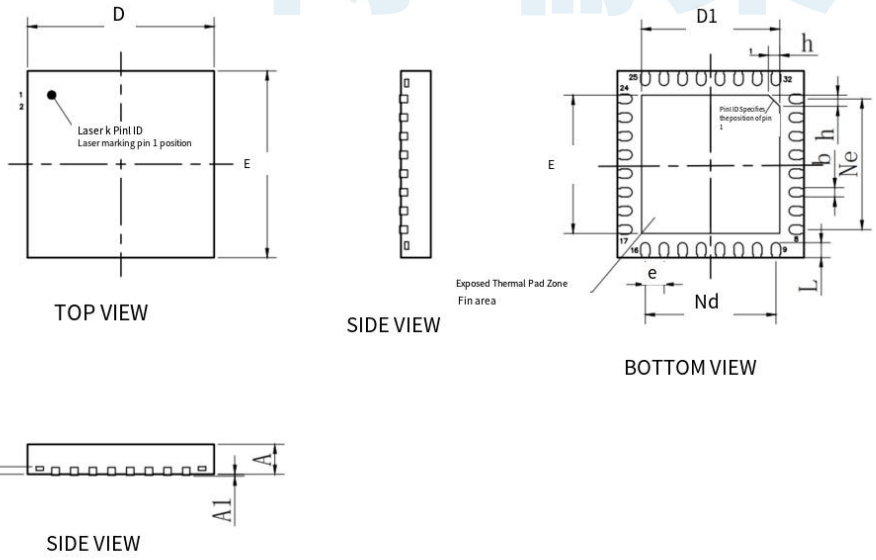


PCB



50 ohms Impedance Signal Lines：width=0.53mm,spacing=0.53mm

Package Dimensions (mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.80	0.85
A1	--	0.02	0.05
b	0.20	0.25	0.30
c		0.203REF	
D	4.90	5.00	5.10
D1	3.35	3.40	3.45
e		0.50BSC	
Ne		3.50BSC	
Nd		3.50BSC	
E	4.90	5.00	5.10
E1	3.35	3.40	3.45
L	0.35	0.40	0.45
h	0.25	0.30	0.35