## FEATURES

Output frequency range: 25.5 MHz～3240 MHz

Fractional-N synthesizer

Programmable divide-by-1/2/4/8/16/32/64 output

Power supply: 3.3 V

Programmable dual-modulus prescaler of 4/5 or 8/9

serial interface

Package Option: QFN32

## APPLICATIONS

Wireless infrastructure (W-CDMA, TD-SCDMA, WiMAX, GSM, PCS, DCS, DECT)

Test equipment

Wireless LANs, CATV equipment

Clock generation

## ABSOLUTE MAXIMUM RATINGS

$SDV_{DD}/DV_{DD}$：3.3V

$AV_{DD}/V_P/V_{VCO}$：3.3V

Operating Temperature Range: -55℃~+125℃

Storage Temperature Range: -65℃~+150℃

## GENERAL DESCRIPTION

The BR9177FL allows implementation of fractional-N or integer-N phase-locked loop (PLL) frequency synthesizers if used with an external loop filter and external reference frequency.

The BR9177FL has an integrated voltage controlled oscillator (VCO) with a fundamental output frequency ranging from 1.62 GHz to 3.24 GHz. In addition, divide-by-1/ 2/ 4/ 8/ 16/ 32 or 64 circuits allow the user to generate RF output frequencies as low as 25.5 MHz.

Control of all the on-chip registers is through a simple serial interface. The device operates with a power supply ranging from 3.0 V to 3.6 V and can be powered down when not in use.

## FUNCTIONAL BLOCK DIAGRAM

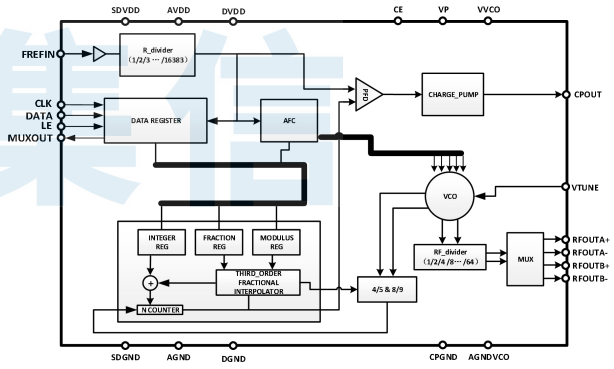



Figure 1.

## ORDERING GUIDE

| Model | Package Option | Description |
|---|---|---|
| BR9177FL | QFN32 | FRACTIONAL-N PLL WITH INTEGRATED VCO |

Table 1.

**SPECIFICATIONS** ( Unless otherwise noted, $SDV_{DD}$=$DV_{DD}$=$AV_{DD}$=$V_P$=$V_{VCO}$=CE=3.3V±10% , $SD_{GND}$=$D_{GND}$ =$A_{GND}$=$CP_{GND}$=$A_{GNDVCO}$=0V. $T_A$= -55℃~+125℃. )

**Table 2.**

| Parameter | | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $REF_{IN}$ CHARACTERISTICS | Input Frequency | | - | - | 600 | MHz |
| | Input Sensitivity | | 0.4 | - | 1.8 | Vp-p |
| PHASE DETECTOR | Phase Detector Frequency | | 7 | - | 26 | MHz |
| CHARGE PUMP | $I_{CP}$ Sink/Source | 0.5V≤CPOUT≤2.8V | 0.025 | - | 6.375 | mA |
| | Sink and Source Current Matching | | - | 1 | - | % |
| | $I_{CP}$ VS. $V_{TUNE}$ | | - | 1.5 | - | % |
| | $I_{CP}$ vs. Temperature | | - | 2 | - | % |
| LOGIC INPUTS | Input High Voltage, $V_{INH}$ | | DVDD-0.4 | - | - | V |
| | Input Low Voltage, $V_{INL}$ | | - | - | 0.4 | V |
| LOGIC OUTPUTS | Output High Voltage,$V_{OH}$ | | DVDD-0.4 | - | - | V |
| | Output Low Voltage, $V_{OL}$ | | - | - | 0.4 | V |
| POWER SUPPLIES | $SDV_{DD}$, $DV_{DD}$, $AV_{DD}$, $V_P$, $V_{VCO}$, CE | - | 3.0 | 3.3 | 3.6 | V |
| | $I_{DD}$ | $REF_{IN}$=20MHz、Prescaler=1、N Division Ratio=100、VCO Output Division Ratio=1 | - | 125 | - | mA |
| RF OUTPUT CHARACTERISTICS | VCO Output Frequency | - | 1620 | - | 3240 | MHz |
| | VCO Sensitivity | - | 60 | - | 126 | MHz/V |
| | Minimum RF Output Power | Temperature: 25℃ RFOUTA+/ RFOUTA- | - | -3 | - | dBm |
| | Maximum RF Output Power | | - | 4 | - | dBm |
| | Minimum VCO Tuning Voltage | - | - | 1.45 | - | V |
| | Maximum VCO Tuning | - | - | 1.85 | - | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | Voltage | | | | | |
| NOISE CHARACTERISTICS | VCO Phase-Noise Performance @1.62GHz | 10 kHz offset | - | -82.3 | - | dBc/Hz |
| | | 100 kHz offset | - | -110.7 | - | dBc/Hz |
| | | 1 MHz offset | - | -133 | - | dBc/Hz |
| | VCO Phase-Noise Performance @3.24GHz | 10 kHz offset | - | -69.3 | - | dBc/Hz |
| | | 100 kHz offset | - | -101.5 | - | dBc/Hz |
| | | 1 MHz offset | - | -128.3 | - | dBc/Hz |
| | PLL Phase-Noise Performance @1.62GHz Phase-frequency Detector: 20MHz Loop Bandwidth: 120KHz | 1 kHz offset | - | -94 | - | dBc/Hz |
| | | 10 kHz offset | - | -102 | - | dBc/Hz |
| | | 100 kHz offset | - | -97 | - | dBc/Hz |
| | | 1 MHz offset | - | -130 | - | dBc/Hz |
| | PLL Phase-Noise Performance @3.24GHz Phase-frequency Detector: 20MHz Loop Bandwidth: 120KHz | 1kHz offset | - | -89 | - | dBc/Hz |
| | | 10 kHz offset | - | -96 | - | dBc/Hz |
| | | 100 kHz offset | - | -91 | - | dBc/Hz |
| | | 1 MHz offset | - | -124 | - | dBc/Hz |
| | PLL Phase-Noise Performance @1620.1MHz Phase-frequency Detector: 20MHz Loop Bandwidth: 40KHz | 1kHz offset | - | -85 | - | dBc/Hz |
| | | 10 kHz offset | - | -86 | - | dBc/Hz |
| | | 100 kHz offset | - | -91 | - | dBc/Hz |
| | | 1 MHz offset | - | -124 | - | dBc/Hz |
| | PLL Phase-Noise Performance @3240.1MHz Phase-frequency Detector: 20MHz Loop Bandwidth: 40KHz | 1kHz offset | - | -80 | - | dBc/Hz |
| | | 10 kHz offset | - | -81 | - | dBc/Hz |
| | | 100 kHz offset | - | -81 | - | dBc/Hz |
| | | 1 MHz offset | - | -120 | - | dBc/Hz |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## TIMING CHARACTERISTICS

（Unless otherwise noted, $SDV_{DD}$=$DV_{DD}$=$AV_{DD}$=$V_P$=$V_{VCO}$=CE=3.3V±10%，$SD_{GND}$=$D_{GND}$ =$A_{GND}$=$CP_{GND}$=$A_{GNDVCO}$=0V. $T_A$= -55 ℃~ 125 ℃. High Voltage: 3.3 V, Low Voltage: 0 V, Timing Frequency $f_{max}$= 25 MHz, T=40 ns. ）

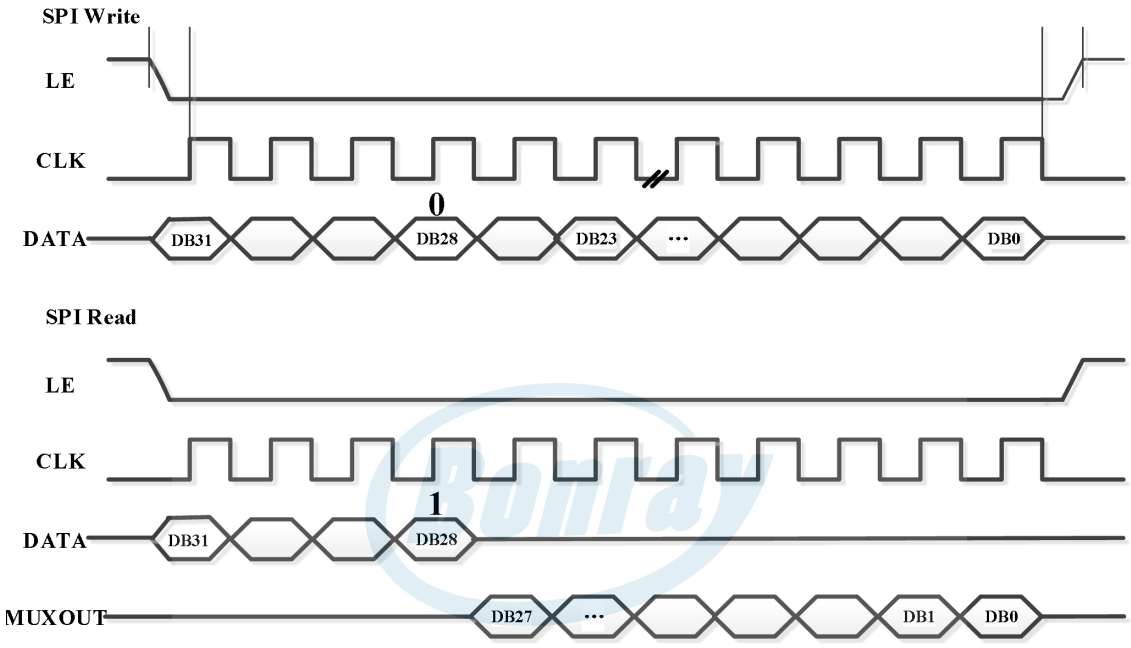



Figure 2. Timing Diagram

**Note**:

1. Register REG0 needs to be configured last, and all register data is refreshed.

2.The first address bit, then read and write bit, the last data bit. The address bit is high first, the data bit is high first.

3. The host sends data along the falling edge, and the slave receives data along the rising edge.

4. SPI speed up to support 25MHz.

5. It is recommended to configure 10 clock edges between registers.

## TYPICAL PERFORMANCE CHARACTERISTICS

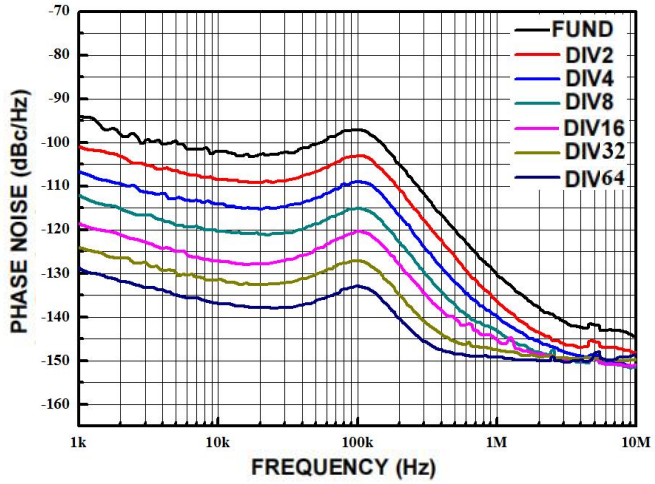



Figure 3. Closed-Loop Phase Noise, Fundamental VCO and Dividers, VCO = 1.62 GHz, Loop Bandwidth =120 kHz

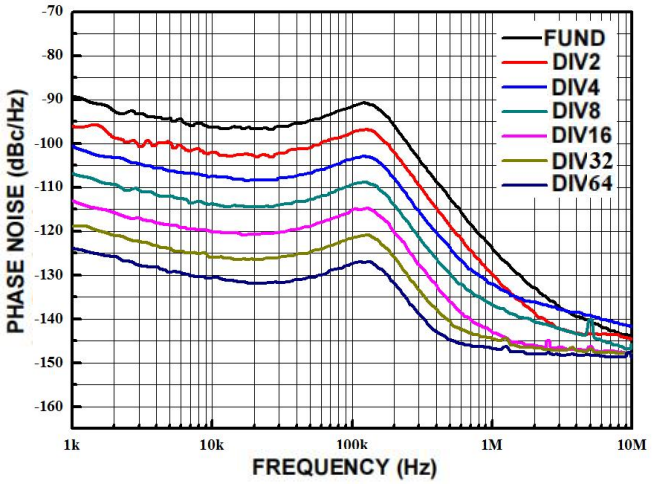



Figure 4. Closed-Loop Phase Noise, Fundamental VCO and Dividers, VCO = 3.24 GHz, Loop Bandwidth =120 kHz

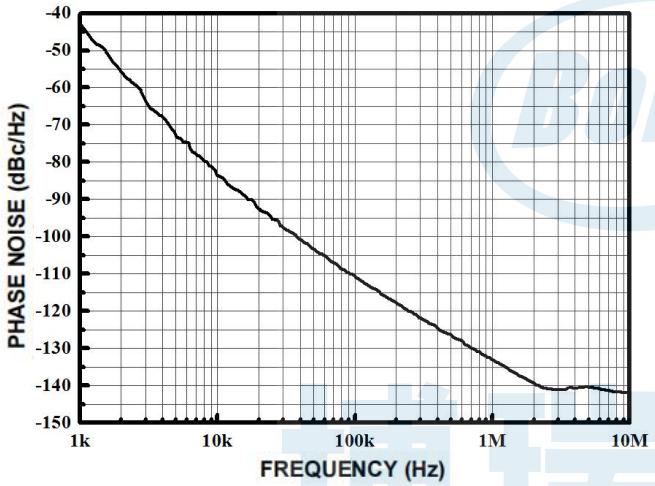



Figure 5. Open-Loop VCO Phase Noise, 1.62 GHz

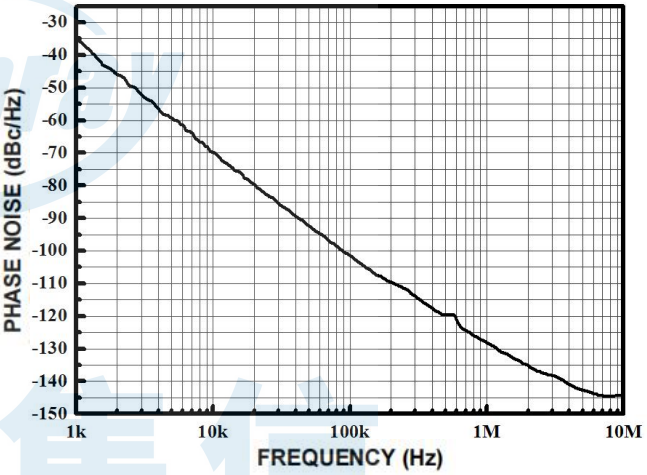



Figure 6. Open-Loop VCO Phase Noise, 3.24 GHz

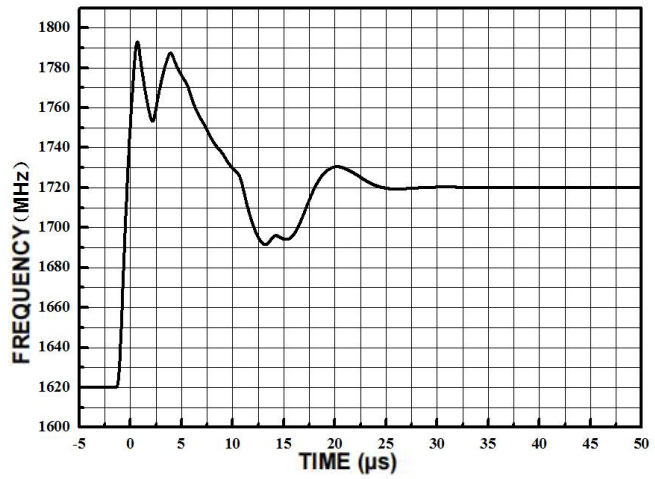



Figure 7. Lock Time for 100 MHz Jump, Loop Filter Bandwidth = 120kHz

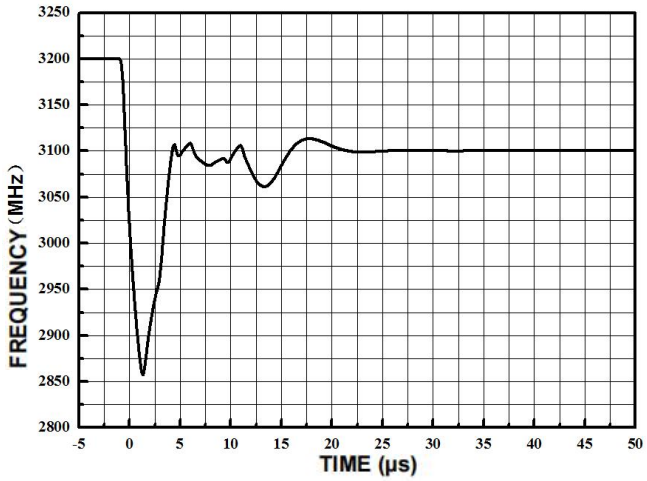



Figure 8. Lock Time for 100 MHz Jump, Loop Filter Bandwidth = 120kHz

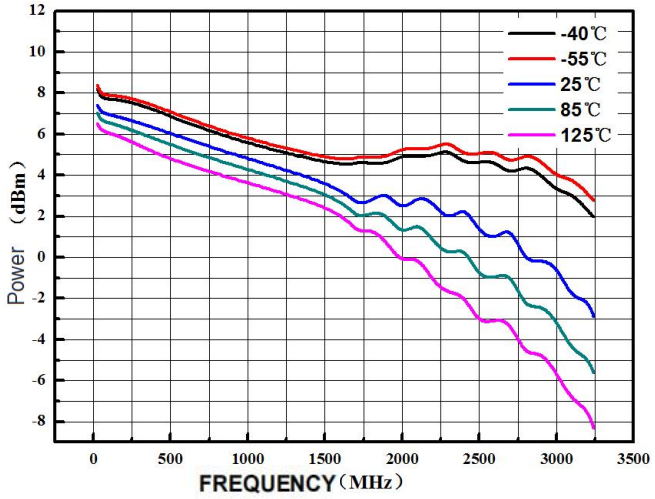



Figure 9. Low Power Mode RFOUTA+/- RF Power

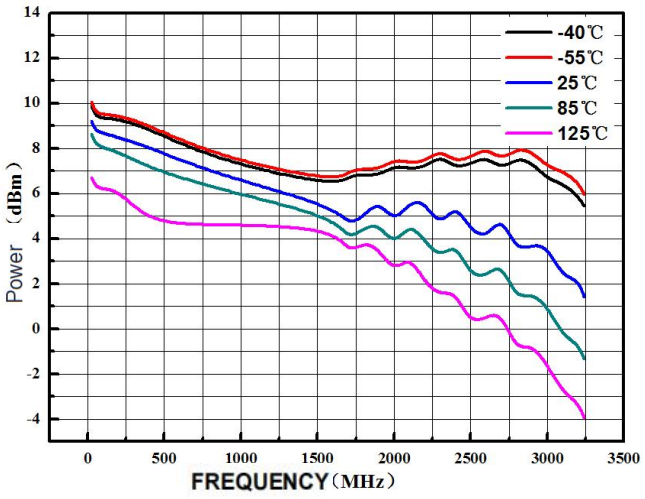



Figure 10. High Power Mode RFOUTA+/- RF Power

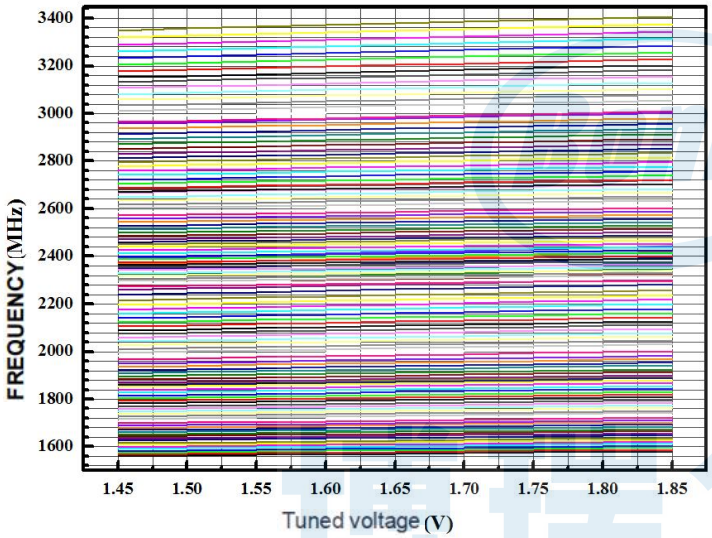
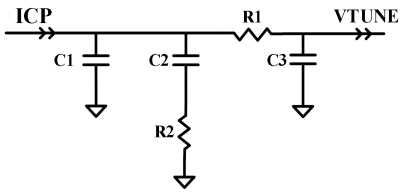



Figure 11. VCO Output Frequency Tuning Curve

**Table 3. Loop Filter Design suggestion**

| Loop Filter Numbering | Loop Filter Bandwidth (KHz) | C1 (pF) | C2 (nF) | C3 (pF) | R1 Ω (k) | R2 Ω (k) | Loop filter Design Reference Drawing |
|---|---|---|---|---|---|---|---|
| 1 | 40 | 8200 | 100 | 1.2 | 20 | 0.12 |  |
| 2 | 80 | 1830 | 33 | 1.2 | 20 | 0.2 | |
| 3 | 120 | 400 | 10 | 1.2 | 20 | 0.32 | |
| 4 | 150 | 1100 | 33 | 1.2 | 20 | 0.47 | |



Note: Loop filter 1 is designed with a phase discriminating frequency of 20MHz and ICP=3.2mA. It is recommended to be applied in decimal mode.Loop filter 3 is designed with 20MHz phase detection frequency and ICP=3.2mA. It is recommended to be applied in integer mode.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

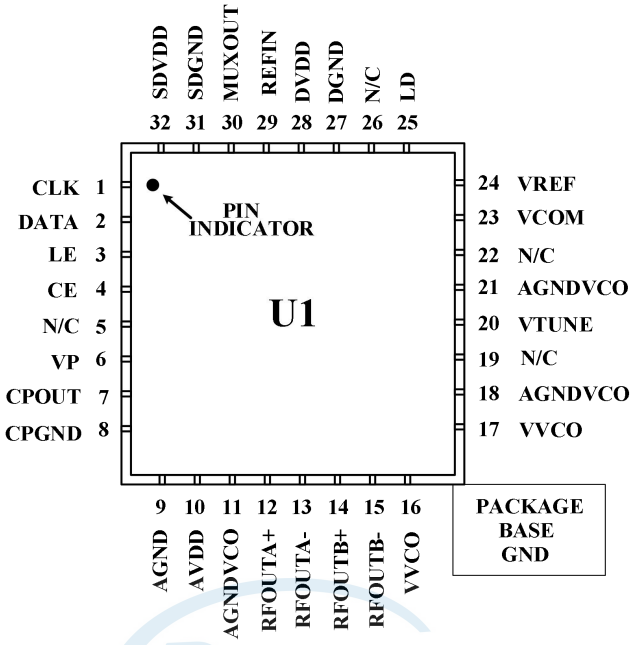



**Figure 12. Pin Configuration**

表 4　引脚说明

| 引脚编号 | 引脚名称 | 描述 |
|---|---|---|
| 1 | CLK | Serial Clock Input |
| 2 | DATA | Serial Data Input |
| 3 | LE | Serial card cable selection |
| 4 | CE | Chip Enable（3.3V） |
| 5、19、22、26 | N/C | Hanging |
| 6 | VP | Analog 3.3V |
| 7 | CPOUT | Charge pump output, this pin provides ±ICP to the outer loop filter, which feeds the outer loop filter into the ICP port |
| 8 | CPGND | Analog Ground |
| 9 | AGND | Analog Ground |
| 10 | AVDD | Analog Power Supply 3.3V |
| 11、18、21 | AGNDVCO | Analog Ground |
| 12 | RFOUTA+ | RF output, The output level is programmable. |
| 13 | RFOUTA- | Complementary RF output, The output level is programmable. |
| 14 | RFOUTB+ | Auxilliary RF Output, output power lower than RFOUTA+, The output level is programmable. |
| 15 | RFOUTB- | Complementary Auxilliary RF Output, output power lower than RFOUTA-, The output level is programmable. |
| 16、17 | VVCO | Analog 3.3V |

| | | |
|---|---|---|
| 20 | VTUNE | Control Input to the VCO.This voltage determines the output frequency and is derived from filtering the VTUNE output voltage. |
| 23 | VCOM | Internal bias port, Decoupling capacitors to the ground plane must be placed as close as possible to this pin. |
| 24 | VREF | Internal bias port, Decoupling capacitors to the ground plane must be placed as close as possible to this pin. |
| 25 | LD(1) | Lock Detect Output Pin. This pin outputs a logic high (3.3 V ) to indicate PLL lock. A logic low output indicates loss of PLL lock. |
| 27 | DGND | Digital Ground. |
| 28 | DVDD | Digital Power Supply 3.3 V |
| 29 | REFIN | Reference Input. External Divider Capacitor |
| 30 | MUXOUT | Multiplexer Output. This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally. |
| 31 | SDGND | Digital Ground. |
| 32 | SDVDD | Digital Power Supply 3.3 V |
| - | EP | Exposed Pad. |

Note: (1) The reference signal RFIN input is required to realize the locking detection function.

## REGISTER MAPS

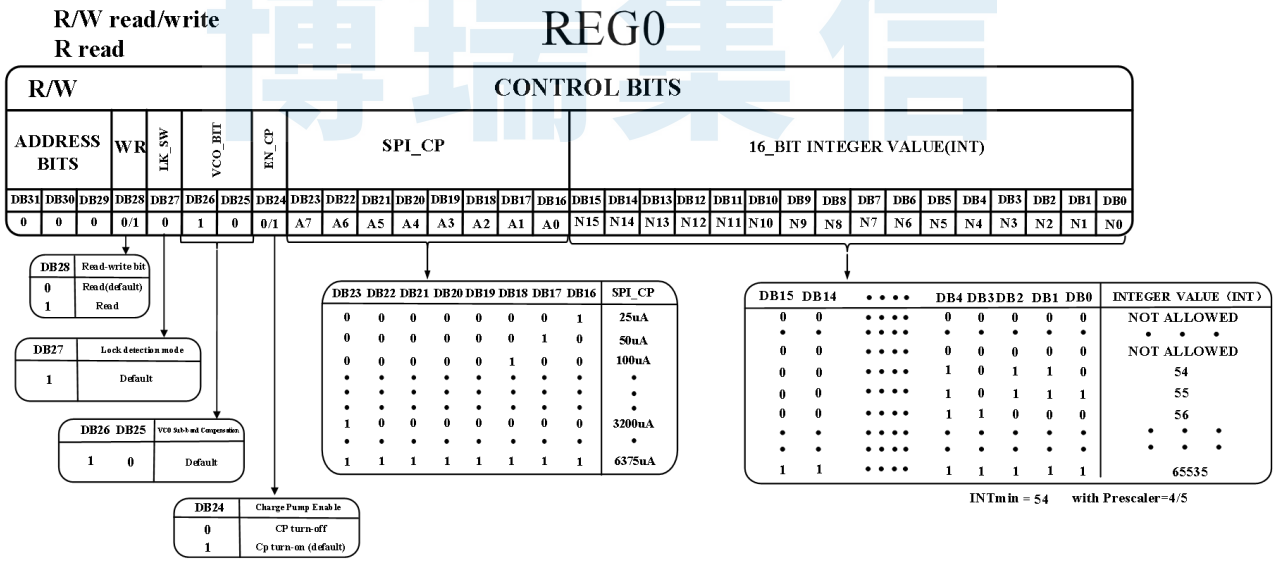



**Figure 13. Register0**

# REG1

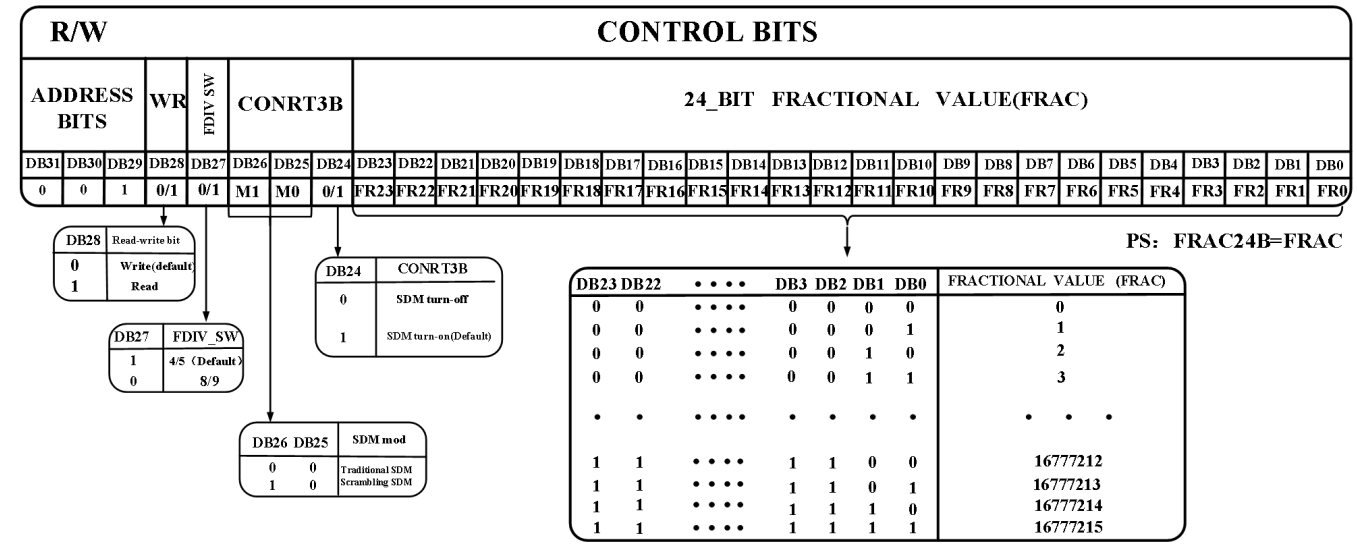



Figure 14. Register1

# REG2

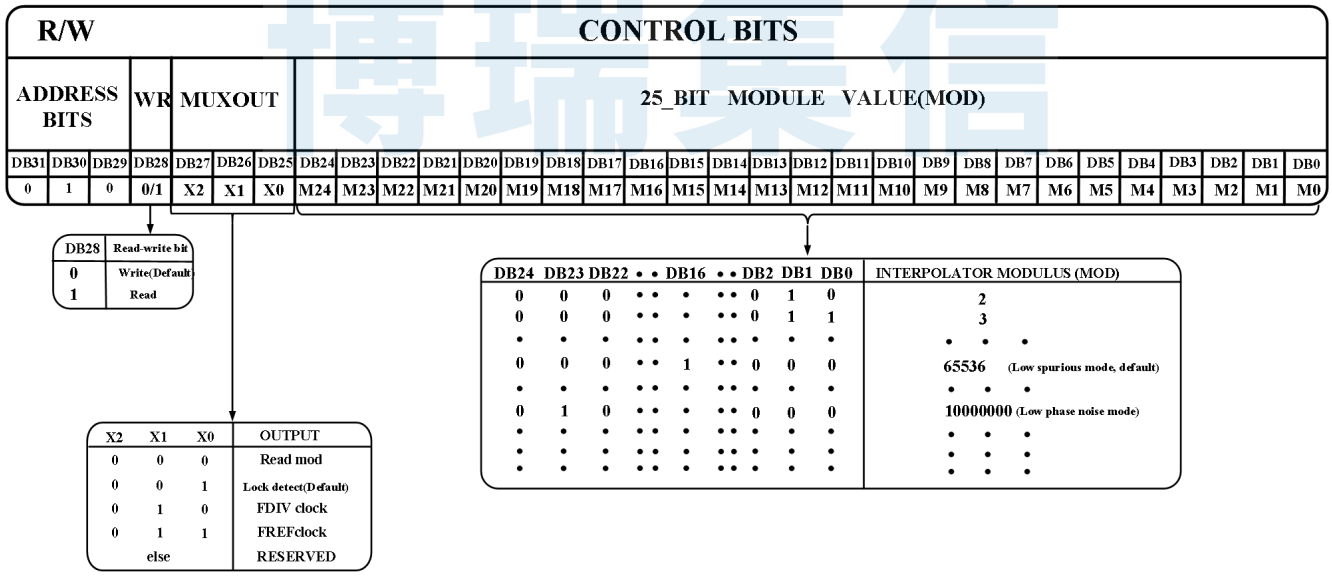



Figure 15. Register2

# REG3

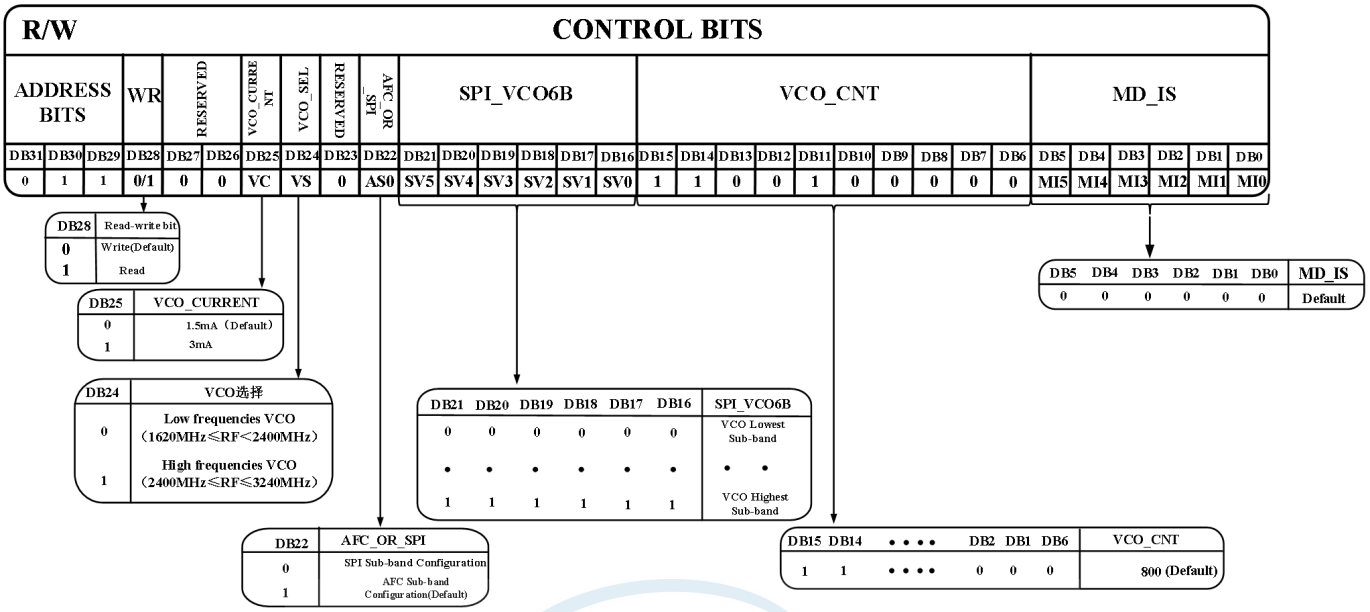



**Figure 16. Register3**

# REG4

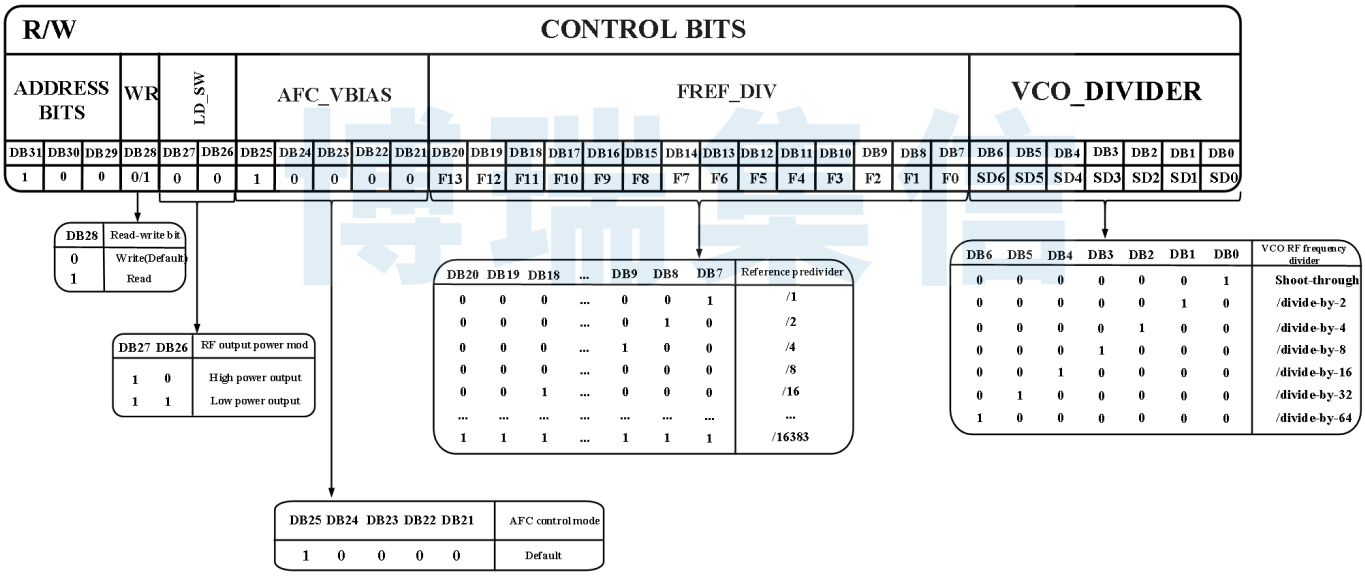



**Figure 17. Register4**

# REG5

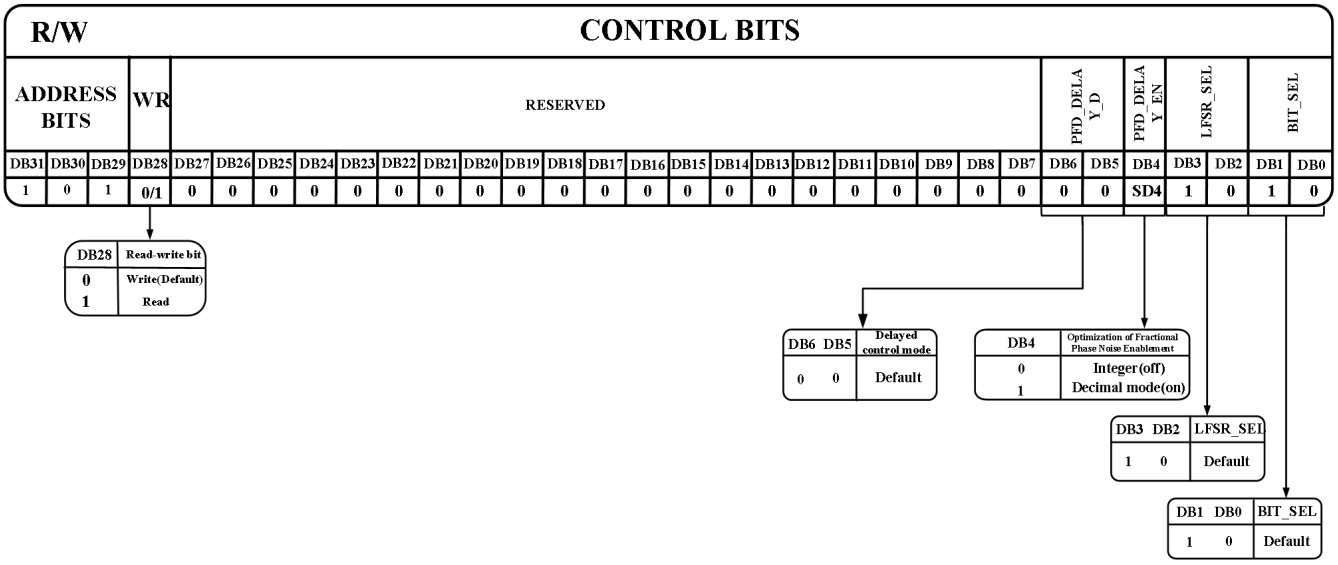



**Figure 18. Register5**

## REGISTER 0

**Control Bits**

With Bits DB[31:29] set to 0, 0, 0, Register 0 is programmed.

**Read/Write Bit**

With Bit DB[28] set to 0, Register 0 can be written.

**Charge Pump Enable Bit**

The charge pump enable bit DB[24] in register 0 is used to control the charge pump current switch. Default charge pump current on DB[24] set to 1.

**Charge Pump Current Set Bit**

The charge pump current setting bit DB[23:16] of register 0 is used to set the charge pump current. The charge pump current should be set to the loop filter's design current of 3.2mA (see Table 2).

**INT Value Set Bits**

The INT setting bit DB[15:0] of register 0 is used to set the INT value, which determines the integer part of the feedback frequency dividing coefficient. Used for formulas $RF_{OUT} = [INT + (FRAC/MOD)] \times [f_{PFD}]/RF\ divider$.

$RF_{out}$ is the RF output frequency, $INT$ is the integer part of the feedback frequency division coefficient, $FRAC/MOD$ is the decimal part of the feedback frequency division coefficient, $f_{PFD}$ is the phase detection frequency, $RF\ divider$ is the VCO radio frequency divider 1~64 frequency division.

## REGISTER 1

**Control Bits**

With Bits DB[31:29] set to 0, 0, 1, Register 1 is programmed.

**Read/Write Bit**

With Bit DB[28] set to 0, Register 1 can be written.

**Prescaler Value Set Bit**

Register 1's prescaler value set bit DB[27] is used to set 4/5 or 8/9. Since the maximum allowable RF frequency of a prescaler value based on synchronous 4/5 division is 3.24GHz, the BR9177FL's full-band setting defaults to 4/5 division.

**SDM Mode and Switch Set Bits**

SDM mode and switch set bit DB[26:24] of register 1 is used to set SDM mode and switch. The SDM switch is on by default, and can be achieved by setting the FRAC molecule value of the decimal input to 0 when the integer frequency is implemented.

**FRAC Set Bit**

The FRAC set bit DB[23:0] of register 1 is used to set the molecular value of the SDM decimal input. It is used in conjunction with the denominator MOD value of the SDM decimal input to achieve the fractional part of the feedback division coefficient.

## REGISTER 2

**Control Bits**

With Bits DB[31:29] set to 0, 1, 0, Register 2 is programmed.

**Read/Write Bit**

With Bit DB[28] set to 0, Register 2 can be written.

**MUXOUT Set Bits**

The MUXOUT set bits DB[27:25] of register 2 is used for either the lock detect, the scaled RF, or the scaled

reference frequency to be accessed externally，with default access lock detection.

**MOD Module Set Bits**

The MOD module set bits DB[24:0] of register 2 is used to set the fractional modulus value of the SDM decimal input. It is used in conjunction with the molecular FRAC value of the SDM decimal input to achieve the fractional part of the feedback frequency division coefficient. When the MOD module is set DB[24:0]= 25 'd10000000, the random sequence of SDM output is more periodic, so the phase noise performance is good, and the decimal stray performance is poor; When MOD module set bit DB[24:0]= 25 'd16777216, SDM output random sequence periodic poor, so the fractional stray performance is better, the phase noise performance is poor.

## REGISTER 3

**Control Bits**

With Bits DB[31:29] set to 0, 1, 1, Register 3 is programmed.

**Read/Write Bit**

With Bit DB[28] set to 0, Register 3 can be written.

**VCO Select Set Bit**

VCO Select Set bit DB[24] of Register 3 is used to select VCO outputs in different RF bands. When 1620MHz is less than or equal to the RF output frequency < 2400MHz, select the low-band VCO. When the RF output frequency is less than or equal to 3240MHz, select the high band VCO.

**AFC or SPI Select Set Bit**

Register 3's AFC or SPI select set bit DB[22] for Select Auto select VCO sub-band or SPI configuration Select sub-band. When DB[22]= 1'b1, the VCO sub-band corresponding to the RF output frequency is automatically selected through the AFC automatic frequency calibration function. When DB[22]= 1 'b0, the SPI is used to manually configure the VCO sub-band corresponding to the RF output frequency. This function must be used together with the VCO sub-band 6bit control bit.

**VCO Sub-band 6bit Control Bits**

The VCO sub-band 6bit control bits DB[21:16] of register 3 is used for the selection of different sub-bands of VCO 64, which needs to be used in conjunction with the AFC or SPI select setting bit. For example, if the RF output frequency is 2GHz and the corresponding low-band VCO sub-band control bit in the table is 6 'b101000, DB[23:22]= 2' b00 and DB[21:16]= 6 'b101000 need to be configured in register 3. When DB[23:22]= 2 'b11, the VCO sub-band 6bit control bits are invalid.

## REGISTER 4

**Control Bits**

With Bits DB[31:29] set to 1, 0, 0, Register 4 is programmed.

**Read/Write Bit**

With Bit DB[28] set to 0, Register 4 can be written.

**RF Output Power Mode Set Bits**

The RF output Power mode set bits DB[27:26] in register 4 is used to select different RF power output modes. When DB[27:26]=11, it is low power RF output mode; When DB[27:26]=10, high power RF output mode.

**Reference Prescaler Set Bits**

The reference prescaler set bit DB[20:7] of register 4 is used to prescale the input reference clock frequency (REFIN) to meet the phase detector input frequency range.

**VCO RF Prescaler Set Bits**

The VCO RF prescaler set bits DB[6:0] of register 4 is used to prescale the RF output frequency by 1 to 64 to achieve a wider band range.

## REGISTER 5

**Control Bits**

With Bits DB[31:29] set to 1, 0, 1, Register 5 is programmed.

**Read/Write Bit**

With Bit DB[28] set to 0, Register 5 can be written.

**Phase Detection Delay Enable Set Bit**

The phase detection delay enable set bit DB[4] of register 5 is used to optimize the fractional mode phase noise, and DB[4] is set to 0 when the frequency division ratio is in integer mode; DB[4] is set to 1 when the frequency division is in decimal mode.

## The sequence of configuration for REGISTER 0~5

When the power pin application place 4.7uF, 0.1uF, 0.01uF capacitors, maximize the interference on the power line filter and power on normal, BR9177FL in accordance with the following register order to complete the configuration:

Register 5→ Register 4→ Register 3→ Register 2→ Register 1→ register 0

**Frequency Point Configuration Instructions**

Here is a Application example of how to configure the BR9177FL:

$$RF_{OUT} = [INT + (FRAC/MOD)] \times [f_{PFD}]/\text{RF divider}$$

$RF_{out}$ is the RF output frequency, $INT$ is the integer part of the feedback frequency division coefficient, $FRAC$ is the fractional frequency division coefficient, and $MOD$ is the modulus, $f_{PFD}$ is the phase detection frequency, $RF\ divider$ is the VCO radio frequency divider 1~64 frequency division.

$f_{PFD} = REFIN \times [1/R]$ REFIN is the reference frequency input, R is the reference prescaler coefficient.

Assume that the existing RF system needs to output frequency of 1620.2MHz ($RF_{OUT}$), the reference crystal (REFIN) frequency of 20MHz, and the frequency channel resolution ($f_{RESOUT}$) of 200KHz.From this we have:

BR9177FL's VCO output frequency 1620 ~ 3240MHz, so RF divider = 1; The output requirement is 200KHz channel resolution( $f_{RESOUT}$), so the VCO output channel resolution is also 200KHz ($f_{RES}$).

MOD =16777216

$f_{PFD} = 20MHz \times [(1)/(1)]$=20MHz

$1620.2 = 20\times [INT + \left(\frac{FRAC}{16777216}\right)]$

Available: INT =81

FRAC= 167772

In the above calculation, the MOD value is 16777216. In the calculation of $f_{PFD}$, the reference divider coefficient R is 1. The value of $f_{PFD}$ here can be set flexibly, but it is less than the maximum frequency of the PFD.

## APPLICATIONS INFORMATION

Figure 19. shows the Typical Application Schematic of BR9177FL. The chip uses 3.3V power supply for Supply Voltage. It is recommended to use MAXIM LDO MAX8902B for Supply Voltage, which will not worsen the noise performance of BR9177FL. External loop filter is required for chip operation, and it is recommended to use a 3-order loop filter. The input reference signal needs to be provided by an external crystal oscillator. Epson TG5032SCN TCXO is recommended for reference input.

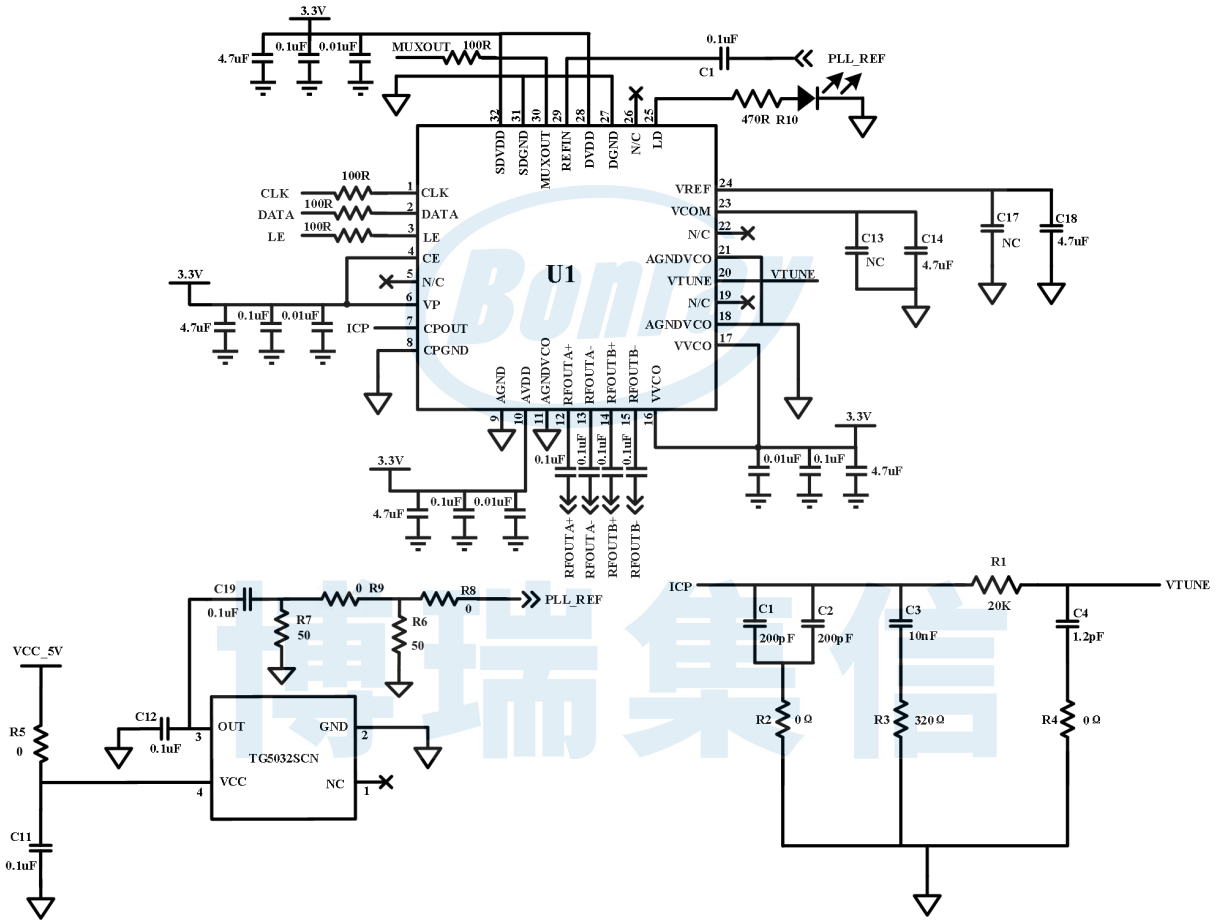
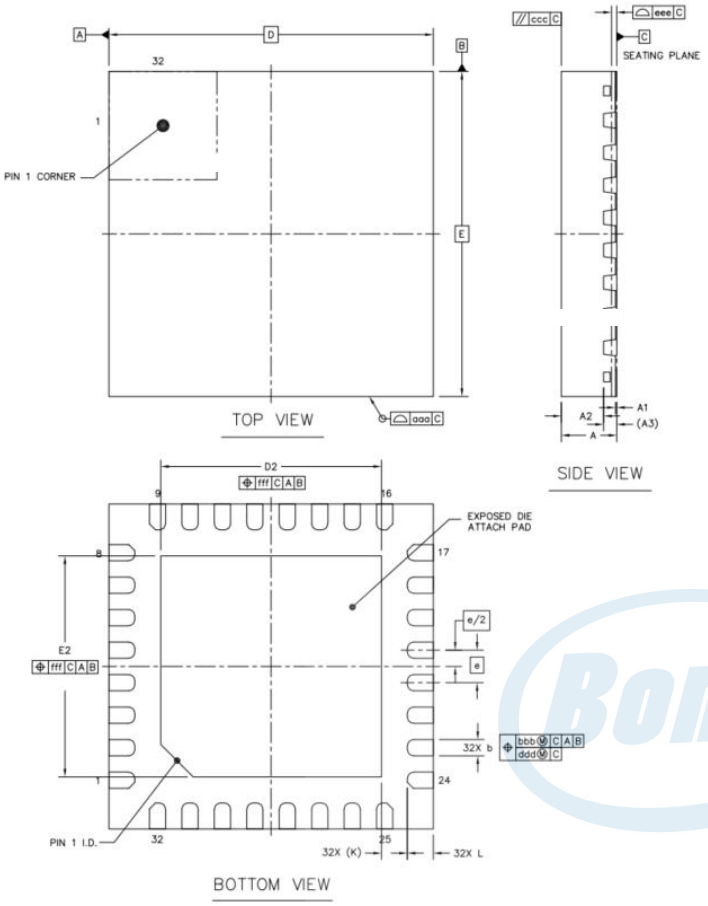



**Figure 19. Direct Conversion Modulator**

## OUTLINE DIMENSIONS (Unit: mm)




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.8 | 0.85 | 0.9 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.65 | --- |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.2 | 0.25 | 0.3 |
| BODY SIZE | X | D | | 5 BSC | |
| | Y | E | | 5 BSC | |
| LEAD PITCH | | e | | 0.5 BSC | |
| EP SIZE | X | D2 | 3.3 | 3.4 | 3.5 |
| | Y | E2 | 3.3 | 3.4 | 3.5 |
| LEAD LENGTH | | L | 0.3 | 0.4 | 0.5 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | | 0.4 REF | |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | ccc | | 0.1 | |
| COPLANARITY | | eee | | 0.08 | |
| LEAD OFFSET | | bbb | | 0.1 | |
| | | ddd | | 0.05 | |
| EXPOSED PAD OFFSET | | fff | | 0.1 | |

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP • Sn8~20s

**Figure 20. Lead Frame Chip Scale Package [LFCSP]**